Switch logic

- Can implement Boolean formulas as networks of switches.
- Can build switches from MOS transistors—transmission gates.
- Transmission gates do not amplify but have smaller layouts.

Behavior of n-type switch

n-type switch has source-drain voltage drop when conducting:
- conducts logic 0 perfectly;
- introduces threshold drop into logic 1.

Types of switches

- Complementary
- N-type

n-type switch driving static logic

Switch underdrives static gate, but gate restores logic levels.
Behavior of complementary switch

- Complementary switch products full-supply voltages for both logic 0 and logic 1:
  - n-type transistor conducts logic 0;
  - p-type transistor conducts logic 1.

Layout characteristics

- Has two source/drain areas compared to one for inverter
- Doesn’t have gate capacitance

Pseudo-nMOS (Ratioed logic)

- Uses a p-type as a resistive pullup, n-type network for pulldowns.

Characteristics

- Consumes static power
- Has much smaller pullup network than static gate
- Pulldown time is longer because pullup is fighting
- Reduced noise margin
  - Compared to SCMOS
- Low-level logic depends on transistor sizes

Output voltages

- Logic 1 output is always at $V_{DD}$
  - $V_{OH} = V_{DD}$
- Logic 0 output is above $V_{SS}$
  - $V_{OL} > V_{SS}$
- $V_{OL} = 0.1(V_{DD} - V_{SS})$ is one plausible choice

Producing output voltages

- For logic 0 output, pullup and pulldown form a voltage divider.
- Must choose n, p transistor sizes to create effective resistances of the required ratio
- Effective resistance of pulldown network must be computed in worst case
  - Series n-types means larger transistors
Transistor ratio calculation

- In steady state logic 0 output ($V_{in}=V_{DD}$):
  - NMOS linear
  - PMOS saturated
  - A mistake in the textbook
- Pullup and pulldown have same current flowing through them

Transistor ratio, cont’d.

- Equate two currents:
  - $I_{dp}=I_{dd}$
  - $V_{OL}$ is proportional to $(W_p/L_p)/(W_n/L_n)$
    - This means to have small $V_{OL}$, we should use smaller pull-up
      - But smaller pulldown $\Rightarrow$ longer rise time
    - $V_{OL}>V_{tn} \Rightarrow$ pulldown network always on!

Why to Use Pseudo-nMOS?

- Pseudo-NMOS vs. SCMOS
  - More power consumption compared to SCMOS
  - Slower than SCMOS
- Why to Use Pseudo-nMOS?
  - Where size and complexity of PU network is a main concern
    - And speed and power consumption less important
  - Applications: busses and PLAs
  - Much less routing compared to SCMOS

DCVS logic

- DCVSL = differential cascode voltage logic
- Static logic—consumes no dynamic power
- Uses latch to compute output quickly
- Requires true/complement inputs
  - Produces true/complement outputs

DCVS structure

DCVS operation

- Exactly one of true/complement pulldown networks will complete a path to the power supply
- Pulldown network will lower output voltage, turning on other p-type, which also turns off p-type for node which is going down.
**Precharged logic**

- Precharged logic vs. SCMOS
  - Lower area and higher speed
  - More complexity in design
    - Operate in two phase
- Take advantage of higher speed of n-types

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**Domino logic**

- Uses precharge clock to compute output in two phases:
  - Precharge
  - Evaluate
- Is not a complete logic family—cannot invert

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**Domino phases**

- Controlled by clock $\phi$.
- **Precharge**: p-type pullup precharges the storage node; inverter ensures that output goes low.
- **Evaluate**: storage node may be pulled down, so output goes up.
Domino buffer (Cont.)

- Inverting buffer isolates storage node
  - Storage node and inverter have correlated values

Domino operation

- Gate outputs fall in sequence:
  - gate 1
  - gate 2
  - gate 3

Domino effect

- Domino gates inputs must be monotonically increasing
  - Glitch causes storage node to discharge

Monotonicity

- Charge can be stored in source/drain connections between pulldowns
- Stored charge can be sufficient to affect precharge node
- Can be averted by precharging the internal pulldown network nodes along with the precharge node.

Using domino logic

- Can rewrite logic expression using De Morgan’s Laws:
  - \((a + b)' = a'b'\)
  - \((ab)' = a' + b'\)
- Add inverters to network inputs/outputs as required

Domino and stored charge

- Charge can be stored in source/drain connections between pulldowns
- Stored charge can be sufficient to affect precharge node
- Can be averted by precharging the internal pulldown network nodes along with the precharge node.
Low-Power Gates

- Leakage power may become a big problem in 1G-transistor designs
- Solutions:
  - Architecture-driven voltage scaling
    - Power consumption is quadratically reduced with voltage scaling
    - Replicate logic to make up for slower operating speeds
  - Use power-supply-controlled gates
    - Turning off gates when they are not in use
  - Multiple-threshold logic