1) Implement each of the following functions with only one Decoder and one NAND gate:
   a) \( F_1 = x'y' + yz + x'yz' + xy'z' \)
   b) \( F_2(x,y,z) = \Sigma(1,2,3,6,7) \)
   c) \( F_3(A,B,C,D) = \Sigma(2,9,10,12,13) + d(1,5,14) \)

2) Implement each of the following functions with only one 4x1-Multiplexer and minimum number of NAND gates:
   a) \( F_4 = AB' + ABD + A'CD' + A'BC' \)
   b) \( F_5(A,B,C,D) = \Sigma(2,9,10,12,13) \)

3) Implement each of the following functions with only one 8x1-Multiplexer and minimum number of NOT gates:
   a) \( F_6 = x'y'w + yz + x'yzw' + xy'z' \)
   b) \( F_7(x,y,z,w) = \Sigma(1,2,4,6,7,12,15) \)
   c) \( F_8(A,B,C,D) = \Sigma(2,8,10,12,14) + d(1,5,13) \)

4) Using one 3x8-Decoder and required gates to implement a circuit for error detection and error correction of a 7-bit Hamming code.