Assignment 1 (Systolic Array)

In computer architecture, a systolic array is a pipe network arrangement of processing units called cells. It is a specialized form of parallel computing, where cells compute data and store it independent of each other.

A systolic array is composed of matrix-like rows of data processing units. Each cell shares the information with its neighbours immediately after processing. The systolic array is often rectangular where data flows across the array between neighbour DPUs, often with different data flowing in different directions.

An example of a systolic algorithm might be designed for matrix multiplication. One matrix is fed in a row at a time from the top of the array and is passed down the array; the other matrix is fed in a column at a time from the left hand side of the array and passes from left to right. Dummy values are then passed in until each processor has seen one whole row and one whole column. At this point, the result of the multiplication is stored in the array and can now be output a row or a column at a time, flowing down or across the array.

In this assignment you are supposed to implement a systolic multiplier. The structure and timing of feeding the network of DUPs is shown below.
Alignments in time

$T = 2$

Alignments in time

$T = 3$

Alignments in time

$T = 4$
Deadline:
Monday 10/31/2011

Important notices:

- DUP block should be implemented in gate level.
- If any other block is needed, it should be implemented in gate level and you are not allowed to use library functions.
- Multiplier size should be defined as a parameter.
- You should learn how to write and use testbench in VHDL.
- The top module process name should be in this format: SYSTOLIC_stdid where stdid is the student number. Also, testbench has to be included and named in SYSTOLIC_bench_stdid.
- Put all the files (testbench included) in a folder named SYSTOLIC_stdid in a zipped format.

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