Disadvantages of Two Stage Combinational Logic XOR Gate

The disadvantage of using the two stage combinational logic XOR gate of Figure 24.22a is that the propagation delay for two gate stages is twice that of one gate stage.

Alternate XOR Implementations

The next chapter on CMOS special purpose gates presents several alternate methods for constructing XOR gates using the logic elements to be presented in that chapter.
24.11 What logic function is performed by the CMOS digital circuit in Figure P24.117?

24.12 What logic function is performed by the CMOS digital circuit in Figure P24.127?

24.13 Calculate the total channel area for a symmetric two-input CMOS NAND gate using (a) \( W_{NMOS} = 4 \mu m \times 2 \mu m \) for the NMOS transistors (b) \( W_{PMOS} = 4 \mu m \times 2 \mu m \) for the PMOS transistors.

24.14 Repeat Problem 24.13 for a three-input CMOS NAND gate.

24.15 Repeat Problem 24.13 for a four-input CMOS NAND gate.

24.16 What logic function is performed by the CMOS complex logic gate in Figure P24.167?

24.17 Modify the gate of Figure P24.16 to provide the inverse of the function it currently performs.

24.18 What logic function is performed by the CMOS complex logic gate in Figure P24.187?

24.19 Figure P24.19 shows the NMOS pull-down section of a six-input complex CMOS logic gate. What logic function is performed by this circuit? Draw the complementary PMOS pull-up section to complete the circuit.

24.20 What logic function is performed by the CMOS gate in Figure P24.217?

24.21 What logic function is performed by the CMOS complex logic gate in Figure P24.217.

24.22 Modify the gate of Figure P24.21 to provide the inverse of the function it currently performs.

24.23 What logic function is performed by the CMOS complex logic gate in Figure P24.237.

24.24 What logic function is performed by the CMOS complex logic gate in Figure P24.247.

24.25 Sketch the CMOS circuit that performs the logic function

\[ F = \overline{A} \overline{B} + C + \overline{D} \]
24.31 What logic function is performed by the CMOS complex logic circuit of Figure P24.31?

24.32 What logic function is performed by the CMOS complex logic circuit of Figure P24.32?

24.33 Design a CMOS complex logic circuit that performs the logical function
\[ F = AB + CD + E + FGH \]
(Design for logic only, don't design the W/L ratio)

24.34 Design a CMOS complex logic circuit that performs the logical function
\[ F = ABC + D + EFG + H \]
and
\[ \overline{F} = ABC + D + EFG + H \]
(Design for logic only, don't design the W/L ratio)

24.35 Design a CMOS complex logic circuit that performs the logical functions
\[ F = ABC + DEF + GH + IJK \]
and
\[ \overline{F} = ABC + DEF + GH + IJK \]
(Design for logic only, don't design the W/L ratio)

24.36 Design a CMOS complex logic circuit that performs the logical function
\[ F = (A + B)C + DEF + F + (G + H)I + J \]
and
\[ \overline{F} = (A + B)C + DEF + F + (G + H)I + J \]
(Design for logic only, don't design the W/L ratio)

24.37 Design a CMOS complex logic circuit that performs the logical function
\[ F = (A + B)(C + D + E + F + I + J) + (G + H) \]
22.12 Draw a three input linear enhancement-only loaded NMOS NAND gate.

22.13 Calculate the output low voltage for the NMOS NAND gate of Figure P22.13. Use $V_{DD} = 1$ V for each stacked pull-down MOSFET. $V_{DD} = -1$ V for the isolated MOSFET, and $k' = 20 \mu A/V^2$ for all transistors. Also, use $(W/L)_{n} = 10 \mu m/5 \mu m$ for each stacked NMOS and $(W/L)_{p} = 5 \mu m/5 \mu m$ for the load NMOS.

22.14 Repeat Problem 22.13 for $k' = 30 \mu A/V^2$.

22.15 Calculate the static power dissipation for the three NMOS NAND gate of Problem 22.13.

22.16 Calculate the output low voltage for the NMOS NAND gate from Figure P22.16. Use $V_{DD} = 1$ V and $k' = 20 \mu A/V^2$ for all transistors. Also, $(W/L)_{n} = 10 \mu m/5 \mu m$ and $(W/L)_{p} = 5 \mu m/5 \mu m$.

22.17 Repeat Problem 22.16 for $k' = 30 \mu A/V^2$.

22.18 Design a two input enhancement-depletion loaded NMOS NAND gate.

22.19 Repeat Problem 22.18 for a three input NAND gate and an output low voltage of $V_{OL} = 0.1$ V.

22.20 (a) Design a two-input enhancement-depletion loaded NMOS NAND gate to have an output low voltage of $V_{OL} = 0.09$ V. Use $V_{DD} = 1$ V for the output transistors, $V_{DD} = -1$ V for $k' = 20 \mu A/V^2$ for all transistors. Use $V_{DD} = 5$ V and any reasonable channel length for the output transistors.

(b) Repeat part (a) for a three input AND gate. Is there a difference?

22.21 What logic function is performed by the NMOS complex logic gate in Figure P22.21? Draw the circuit symbol for this logic gate.

22.22 What logic function is performed by the NMOS complex logic gate in Figure P22.22? Draw the circuit symbol for this logic gate.

22.23 Draw the circuit symbol for the logic gate $F = AB + C + DE$.
22.39 What logic function is performed by the digital circuit of Figure 22.40? Draw the circuit symbol for this logic gate.

22.40 What logic function is performed by the digital circuit of Figure 22.41? Draw the circuit symbol for this logic gate.

22.41 Modify the circuit of Figure 22.39 so that it performs the logic functions:
\[ F = (A + B)C + D(E + F) + (C + H)H + I \]
and
\[ F = (A + B)(C + D) + E + F + (G + H)H + I \]

Draw the circuit symbol for this logic gate.

22.42 Modify the circuit of Figure 22.40 so that it performs the logic function:
\[ F = (A + B)(C + D) + E + F + (G + H)H + I \]

and draw the circuit symbol for this logic gate.

22.43 Design an NMOS complex logic circuit that performs the logic functions:
\[ F = (A + B)(C + D)(E + F) + (G + H)H + I \]

and
\[ F = (A + B)(C + D)(E + F) + (G + H)H + I \]

Draw the circuit symbol for this logic gate. (Design for logic only; don't design the W/L ratios)

22.44 Design an NMOS complex logic circuit that performs the logical function:
\[ F = (A + B)(C + D)(E + F) + (G + H)H + I \]

Draw the circuit symbol for this logic gate. (Design for logic only; don't design the W/L ratios)

22.45 What logic function is performed by the NMOS logic circuit of Figure 22.45? Is there any redundant logic in this circuit?