

## Saba Ahmadian Khameneh

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### RESEARCH INTERESTS

- Storage Systems Design
- Virtualized Platforms
- Fault Tolerant Design
- Low Power Systems Design

### EDUCATION

**Doctor of Philosophy**, in Computer Engineering in Sharif University of Technology, Tehran, Iran.

[GPA: 18.36/20]

2015-now

**Thesis:** “*Improving Efficiency of Storage Subsystems for Virtualization Platforms*”, under supervision of Dr. Hossein Asadi.

**Master of Science**, in Computer Architecture in Sharif University of Technology, Tehran, Iran.

[GPA: 18.80/20]

2013-2015

**Thesis:** “*Development of a Reliability Aware Energy Management Technique for Automata-Based Embedded Systems*”, under supervision of Dr. Alireza Ejlali.

**Bachelor of Science**, in Computer Engineering in Sharif University of Technology, Tehran, Iran. With major in Computer Hardware Engineering.

[GPA: 17.1/20, Major: 19.1/20]

2009-2013

**Thesis:** “*A study on Fully Adiabatic families to compare their reliability, performance and power consumption*”, under supervision of Dr. Alireza Ejlali.

### PATENTS

- Hossein Asadi and **Saba Ahmadian**, “A High-Endurance and Cost-Efficient I/O Caching Scheme for Virtualized Platforms”, US Patent, Application Pending, Feb. 2018. (Initial approval by [patentoffice.ir](http://patentoffice.ir)).

### PUBLICATIONS

- **Saba Ahmadian**, Reza Salkhordeh, and Hossein Asadi, “*LBICA: A Load Balancer for I/O Cache Architectures*”, IEEE/ACM Design, Automation and Test in Europe Conference (DATE), Florence, Italy, March 2019.
- **Saba Ahmadian**, Farhad Taheri, Mehrshad Lotfi, Maryam Karimi, and Hossein Asadi, “*Investigating Power Outage Effects on Reliability of Solid-State Drives*”, IEEE/ACM Design, Automation and Test in Europe Conference (DATE), Dresden, Germany, March 2018.
- **Saba Ahmadian**, Onur Mutlu, and Hossein Asadi, “*ECI-Cache: A High-Endurance and Cost-Efficient I/O Caching Scheme for Virtualized Platforms*”, ACM SIGMETRICS, Irvine, California, June 2018 (Proceedings will be published in a special issue by ACM POMACS).
- Mohammad K. Tavana, **Saba Ahmadian**, and Maziar Goudarzi, “*Dynamically Adaptive Register File Architecture for Energy Reduction in Embedded Processors*”, Elsevier Microprocessors and Microsystems, Jan. 2015.

## HONORS AND AWARDS

- Member of **Iran's National Elites Foundation (INEF)**.
- Qualified to graduate studies (PhD) in **Sharif University of Technology** without entrance exam, 2015.
- Qualified to graduate studies (MSc) in **Sharif University of Technology** without entrance exam, 2013.
- Ranked in top 10 students in cumulative GPA of the Computer Engineering (Hardware), 2009 beginners, **Sharif University of Technology**.
- Ranked 134<sup>th</sup> among more than 300,000 students in annual nationwide universities entrance exam of Iran 2009.

## TECHNICAL EXPERIENCE

- Technical Manager at High Performance Data Storage (HPDS) Corp. (2017-now).
- Expert at High Performance Data Storage (HPDS) Corp. (2014-2017).
- Expert at High Performance Computing Center (HPCC) in Sharif University of Technology (2014-2015).

## RESEARCH EXPERIENCE

- Member of Data Storage and Network Laboratory (DSN-Lab) under supervision of Dr. Hossein Asadi (2015-now).
- Member of Embedded Systems Research Laboratory (ESRLab) under supervision of Dr. Alireza Ejlali (2012-2015).
- Member of Energy Aware Systems Laboratory (EASY) under supervision of Dr. Maziar Goudarzi (2011-2012).

## NOTABLE COURSE PROJECTS

- **Implementing a Fault Injection and Failure Detection Platform for Storage Subsystems:** Advanced Storage Systems course project.
- **Implementing DFT (Design For Testability) Techniques in Complex Digital Systems:** Testability course project.
- **Research about Implemented Fault Tolerance Techniques in FPGAs:** Fault tolerant systems design course project.
- **Investigating Architectural Parameters for Optimizing Power in FPGAs:** Reconfigurable computing course project, by taking advantage from VPR tool.
- **Developing a Standard 250nm Cell Library (including .lib, .v, .lef, .tlf files):** VLSI course project.
- **Developing a Regular Expression Parser on Cell BE Processor:** Microprocessor course project, developed in C in addition to taking full advantage of Cell BE's intrinsic and multi core structure.
- **Implementing Tetris Game on Altera DE2 FPGA:** Digital Systems Design course project, developed in Verilog.

- **Developing a High Performance, Low Power Dynamic Random Access Memory (DRAM):** Digital Electronics course project, developed by Hspice.
- **Design and Implementation of schematic Pipeline MIPS processor:** Computer Architecture course project, developed by Quartus.
- **Design and Implementation of schematic Single Cycle MIPS processor:** Computer Architecture course project, developed by Quartus.
- **Implementing Digital Circuits Developer:** Advanced Programming course project, developed in C++.
- **Implementing Checkers Game:** Fundamental of Programming course project, developed in C.

## SKILLS

- **Project Management:** Jira, MS Project
- **Storage Systems:** DELL EMC<sup>2</sup> VNX Series, HPDS SAB Series
- **Virtualization Platforms:** ESXi, XEN, QEMU
- **Clustering:** Rocks Cluster Distribution
- **PROG. LANGUAGES:** Proficient in Java, C/C++, MATLAB
- **HDL:** Verilog
- **Operating Systems:** Linux, Mac OS, Windows
- **MODELING and SIMULATIONS:** Modelsim, Hspice, Pspice, Tspice, Altium Designer
- **SYNTHESIZE TOOL:** Synopsys Design Compiler(+Power Compiler), Altera Quartus II, Xilinx ISE, Tanners EDA LEdit, SEdit, Virtuoso
- **BACK-END:** Cadence SoC Encounter
- **PROCESSOR and FPGA ARCHITECTURE:** OpenRISC1200, MIPS, Xilinx Virtex Family
- **ARCHITECTURAL SIMULATION:** or1kSim(OpenRISC1200)
- **LANGUAGE:** Persian(native), Turkish(mother tongue), English(fluent), Arabic(familiar)

## HOBBIES

- **SPORTS:** Volleyball, Ping Pong
- **ART:** Photography

## REFERENCES

**Dr. Hossein Asadi**, Associate Professor, Computer Engineering, SUT.  
asadi@sharif.edu

**Dr. Alireza Ejlali**, Associate Professor, Computer Engineering, SUT.  
ejlali@sharif.edu

**Dr. Siavash Bayat-Sarmadi**, Assistant Professor, Computer Engineering, SUT.  
sbayat@sharif.edu