Saba Ahmadian Khamene

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RESEARCH INTERESTS

- Storage Systems Design
- Virtualization Platforms
- Fault Tolerant Design
- Low Power Systems Design

EDUCATION

Doctor of Philosophy, in Computer Engineering in Sharif University of Technology, Tehran, Iran.
[GPA: 18.36/20] 2015-now
Thesis: *"Improving Efficiency of Storage Subsystems for Virtualization Platforms"*, under supervision of Dr. Hossein Asadi.

Master of Science, in Computer Architecture in Sharif University of Technology, Tehran, Iran.
[GPA: 18.80/20] 2013-2015
Thesis: *"Development of a Reliability Aware Energy Management Technique for Automata-Based Embedded Systems"*, under supervision of Dr. Alireza Ejlali.

Bachelor of Science, in Computer Engineering in Sharif University of Technology, Tehran, Iran. With major in Computer Hardware Engineering.
[GPA: 17.1/20, Major: 19.1/20] 2009-2013
Thesis: *"A study on Fully Adiabatic families to compare their reliability, performance and power consumption"*, under supervision of Dr. Alireza Ejlali.

Diploma, in Math and Physics, Nemune Dolati High school, Tabriz, Iran.
[GPA: 19.85/20] 2005-2009

PUBLICATIONS

- Mohammad K.Tavana, **Saba Ahmadian,** Maziar Goudarzi, *"Dynamically Adaptive Register File Architecture for Energy Reduction in Embedded Processors",* accepted, to appear in the Elsevier Microprocessors and Microsystems, Jan. 2015.

HONORS AND AWARDS

- Member of **Iran's National Elites Foundation (INEF)**.
- Qualified to graduate studies (PhD) in **Sharif University of Technology** without entrance exam, 2015.
- Qualified to graduate studies (MS) in **Sharif University of Technology** without entrance exam, 2013.
- Ranked in top 10 students in cumulative GPA of the Computer Engineering (Hardware), 2009 beginners, **Sharif University of Technology**.

- Ranked 134^{th} among more than 300,000 students in annual nationwide universities entrance exam of Iran 2009.

TECHNICAL EXPERIENCE

- Expert at High Performance Data Storage (HPDS) (2014-now).
- Expert at High Performance Computing Center (HPCC) in Sharif University of Technology (2014-2015).

RESEARCH EXPERIENCE

- Member of Data Storage and Network Laboratory (DSN-Lab) under supervision of Dr. Hossein Asadi (2015-now).
- Member of Embedded Systems Research Laboratory (ESRLab) under supervision of Dr. Alireza Ejlali (2012-2015).
- Member of Energy Aware Systems Laboratory (EASY) under supervision of Dr. Maziar Goudarzi (2011-2012).

NOTABLE COURSE PROJECTS

- **Implementing a Fault Injection and Failure Detection Platform for Storage Subsystems:** Advanced Storage Systems course project.
- **Implementing DFT (Design For Testability) Techniques in Complex Digital Systems:** Testability course project.
- **Research about Implemented Fault Tolerance Techniques in FPGAs:** Fault tolerant systems design course project.
- **Investigating Architectural Parameters for Optimizing Power in FPGAs:** Reconfigurable computing course project, by taking advantage from VPR tool.
- **Developing a Standard 250nm Cell Library (including .lib, .v, .lef, .tlf files):** VLSI course project.
- **Developing a Regular Expression Parser on Cell BE Processor:** Microprocessor course project, developed in C in addition to taking full advantage of Cell BE's intrinsic and multi core structure.
- **Implementing Tetris Game on Altera DE2 FPGA:** Digital Systems Design course project, developed in Verilog.
- **Developing a High Performance, Low Power Dynamic Random Access Memory (DRAM):** Digital Electronics course project, developed by Hspice.
- **Design and Implementation of schematic Pipeline MIPS processor:** Computer Architecture course project, developed by Quartus.
- **Design and Implementation of schematic Single Cycle MIPS processor:** Computer Architecture course project, developed by Quartus.

- **Implementing Digital Circuits Developer:** Advanced Programming course project, developed in C++.

- **Implementing Checkers Game:** Fundamental of Programming course project, developed in C.

SKILLS

- **Virtualization Platforms:** ESXi, XEN, QEMU
- **Clustering:** Rocks Cluster Distribution
- **PROG. LANGUAGES:** Proficient in Java, C/C++, MATLAB
- **HDL:** Verilog
- **Operating Systems:** Linux, Mac OS, Windows
- **MODELING and SIMULATIONS:** Modelsim, Hspice, Pspice, Tspice, Altium Designer
- **SYNTHESIZE TOOL:** Synopsys Design Compiler(+Power Compiler), Altera Quartus II, Xilinx ISE, Tanners EDA LEdit, SEdit, Virtuoso
- **BACK-END:** Cadence SoC Encounter
- **PROCESSOR and FPGA ARCHITECTURE:** OpenRISC1200, MIPS, Xilinx Virtex Family
- **ARCHITECTURAL SIMULATION:** or1kSim(OpenRISC1200)
- **LANGUAGE:** Persian(native), Turkish(mother tongue), English(fluent), Arabic(familiar)

HOBBIES

- **SPORTS:** Vollyball, Ping Pong
- **ART:** Photography

REFERENCES

Dr. Hossein Asadi, Associate Professor, Computer Engineering, SUT.
asadi@sharif.edu
Dr. Alireza Ejlali, Associate Professor, Computer Engineering, SUT.
ejlali@sharif.edu
Dr. Siavash Bayat-Sarmadi, Assistant Professor, Computer Engineering, SUT.
sbayat@sharif.edu