Amir Mahdi Hosseini Monazzah

Curriculum Vitae

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DOB: April 21, 1987

Education

2017–Present **Institute for Research in Fundamental Sciences (IPM), Tehran, Iran**, *Post-doc*, *Computer Engineering*, Under Supervision of Prof. Hamid Sarbazi-Azad.

2013–2017 **Sharif University of Technology, Tehran, Iran**, *Phd*, *Computer Engineering*, Under Supervision of Prof. Seyed Ghassem Miremadi.
GPA: 19.38/20

2016–2017 **University of California, Irvine, California, USA**, *Sabbatical*, *Reliable Embedded Systems*, Under Supervision of Prof. Nikil Dutt.

2010–2012 **Sharif University of Technology, Tehran, Iran**, *M.Sc.*, *Computer Architecture*, Under Supervision of Prof. Seyed Ghassem Miremadi.
GPA: 17.91/20

2005–2009 **Islamic Azad University- South-Tehran Branch, Tehran, Iran**, *B.S.*, *Computer Hardware Engineering*, Under Supervision of Mr. Fatehi Khajeh.
GPA: 17.71/20

2001–2005 **Dr. Hesabi High School, Tehran, Iran**, *High School Diploma*, *Mathematics and Physics*.
GPA: 18.8/20

Objective and Major Interests

1. **Test and reliability Challenges of Emerging Non-Volatile Memories**.
2. **Power and Reliability Challenges in Internet of Things (IoT) Applications**.
3. **Reliable Software for Unreliable Hardware**.
4. **Dependable Embedded Systems**.
5. **Reliability Issues in Multi-Core Systems** .

Honors & Awards

1. **Ranked 1^{st} during the PhD program on hardware computer engineering at Sharif University of Technology.**.
2. **Ranked 3^{rd} among about 700 participants in PhD national entrance exam for graduate students in Computer Architecture**.
3. **Ranked 41^{st} among about 15,000 participants in M.Sc. national entrance exam for graduate students in Computer Architecture**.
3. **Ranked 2^{ed} among about 100 students in B.S.**.

Skills & Abilities

Programming Languages	Verilog HDL, VHDL, SystemC, C/C++
Tools	gem5, Cooja, NvSim, CACTI, ModelSim, HDL Designer, Design Compiler, Quartus, MATLAB (m-file programming, Simulink/Stateflow), Cadence SoC Encounter, HSpice
Software	LaTeX, MS Word, MS Excel

Teaching

2018 **Digital Design**, Lecturer, Iran University of science and technology.

2015 **Hardware Laboratory**, Instructor, Sharif University of Technology.

2015 **Advanced Fault-Tolerant System Design**, Teacher Assistant, Sharif University of Technology, Under Supervision of Prof. Seyed Ghassem Miremadi.

2014 **Computer Architecture Laboratory**, Instructor, Sharif University of Technology.

2014 **Fault-Tolerant System Design**, Teacher Assistant, Sharif University of Technology, Under Supervision of Prof. Seyed Ghassem Miremadi.

2013 **Digital Design Laboratory**, Instructor, Sharif University of Technology.

Work Experience

Summer 2008 **Internship**, Iran Khodro Industrial Group, IKCO, Tehran, Iran.
The Complex of Computer Systems Supports and Maintenance

Publications

J-1 **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "OPTIMAS: Overwrite Purging Through In-execution Memory Address Snooping to Improve Lifetime of NVM-based Scratchpad Memories," Accepted for publication in IEEE Transactions on Device and Materials Reliability (TDMR'17).

J-2 Z. Azad, H. Farbeh, **A. M. H. Monazzah**, and A. G. Miremadi, "AWARE: Adaptive Way Allocation for Reconfigurable ECCs to Protect Write Errors in STT-RAM Caches," Accepted for publication in IEEE Transactions on Emerging Topics in Computing (TETC'17).

J-3 Z. Azad, H. Farbeh, **A. M. H. Monazzah**, and A. G. Miremadi, "An Efficient Protection Technique for Last Level STT-RAM Caches in Multi-Core Processors," Accepted for publication in IEEE Transactions on Parallel and Distributed Systems (TPDS'16), vol. 28, no. 6, pp. 1564-1577, June 2017.

J-4 **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "LER: Least Error Rate Replacement Algorithm for Emerging STT-RAM Caches," IEEE Transactions on Device and Materials Reliability (TDMR'16), vol. 16, no. 2, pp. 220-226, June 2016.

C-1 B. Donyanavard, **A. M. H. Monazzah**, T. Muck and N. Dutt, "Exploring Hybrid Memory Caches in Chip Multiprocessors," in proceedings of international symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC'18), Lille, France, July 9-11, 2018.

C-2 B. Safaei, **A. M. H. Monazzah**, T. Shahroodi, A. Faraji, S. Tabaeiaghdaeiand, and A. Ejlali, "The Influence of Objective Functions on Primitive Properties of IoT Infrastructures," to appear in Proceedings of The CSI International Symposium on Real-Time and Embedded Systems and Technologies (RTEST), Tehran, Iran, May 9-10, 2018.

C-3 B. Safaei, **A. M. H. Monazzah**, M. B. Bafroei, and A. Ejlali, "Reliability Side-Effects in Internet of Things Application Layer Protocols," to appear in Proceedings of the IEEE International Conference on System Reliability and Safety (ICSRS'17), Milan, Italy, December 20-22, 2017.

C-4 Z. Azad, H. Farbeh, and **A. M. H. Monazzah**, "ORIENT: Organized Interleaved ECCs for New STT-RAM Caches," to appear in Proceedings of IEEE International Symposium on Design, Automation, and Test in Europe (DATE'18), Dresden, Germany, March 19-23, 2017.

C-5 G. Ghasemi, **A. M. H. Monazzah**, and H. Farbeh, "RI-COTS: Trading Performance for Reliability Improvements in Commercial Of The Shelf Systems," to appear in Proceedings of IEEE International Symposium on Computer Architecture and Digital Systems (CADSÂĂŹ17), Kish Island, Iran, December 21-22, 2017.

C-6 **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "Investigating the Effects of Process Variations and System Workloads on Endurance of NonVolatile Caches," to appear in proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nano technology Systems (DFT'17), Cambridge, United Kingdom, October 23-25, 2017.

C-7 B. Donyanavard, **A. M. H. Monazzah**, T. Muck and N. Dutt, "Work-in-Progress: Exploring Fast and Slow Memories in HMP Core Types," in proceedings of IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'17), Seoul, South Korea, October 15-20, 2017.

C-8 **A. M. H. Monazzah**, M. Shoushtari, S. G. Miremadi, A. M. Rahmani, and N. Dutt, "QuARK: Quality-configurable approximate STT-MRAM Cache by Fine-grained Tuning of Reliability-Energy Knobs ," in proceedings of IEEE proceedings of International Symposium on Low Power Electronics and Designe (ISLPED'17), Taipei, Taiwan, July 24-26, 2017.

C-9 S. Asadi, **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "WIPE: Wearout-Informed Pattern Elimination to Improve the Endurance of NVM based Caches," in Proceedings of the IEEE Asia and South Pacific Design Automation Conference (ASP-DAC'17), Tokyo, Japan, January 16-19, 2017.

C-10 E. Cheshmikhani, **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "Investigating the Effects of Process Variations and System Workloads on Reliability of STT-RAM Caches," to appear in Proceedings of the IEEE European Dependable Computing Conference (EDCC'16), Gothenburg, Sweden, September 5-9, 2016.

C-11 S. G. Ghaemi, **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "LATED: Lifetime-Aware Tag for Enduring Design," in Proceedings of the IEEE European Dependable Computing Conference (EDCC'15), Paris, France, September 7-11, 2015.

C-12 H. Sayadi, H. Farbeh, **A. M. H. Monazzah**, and S. G. Miremadi, "A Data Recomputation Approach for Reliability Improvement of Scratchpad Memory in Embedded Systems," in Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nano technology Systems (DFTÂĂŹ14), Amsterdam, Netherlands, October 1-3, 2014.

C-13 H. M. Makrani, **A. M. H. Monazzah**, H. Farbeh, and S. G. Miremadi, "Evaluation of Sofware-Based Fault-Tolerant Techniques on Embedded OSâĂŹs Components," in Proceedings of the International Conference on Dependability (DEPEND'14), Lisbon, Portugal, November 16-20, 2014.

C-14 **A. M. H. Monazzah**, H. Farbeh, S. G. Miremadi, M. Fazeli, and H. Asadi, "FT-SPM: A Fault-Tolerant ScratchPad Memory," in Proceedings of the Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN'13), Budapest, Hungary, June 24-27, 2013.

Accomplished Projects & Term Papers

2014 **Advanced VLSI Design (Dr. S. Kouhi)**, Exploring The Placement and Routing of ISCAS 89 Circuits Techniques Through SoC Encounter.

2014 **Hardware Security and Trust (Dr. S. Bayat Sarmadi)**, Side Channel Attacks through Acoustic Emanations.

2014 **Electronic System Level Design (Dr. M. Goudarzi)**, Improving The Performance of AES Algorithm Using FPGA-Based Design.

2013 **Low Power Designs (Dr. A. Ejlali)**, Investigation of Determinant Factors of Minimum Operating Voltage of Logic Gates in 65-nm CMOS.

2013 **Advanced Storage Systems (Dr. Hossein Asadi)**, File System Aware Reduction of Write Amplification in SSD Base Storage Systems.

2011 **Reconfigurable Computing (Dr. Hossein Asadi)**, Reducing Hard FIT Rates using Dynamic Reconfiguration.

2011 **Embedded System Design Course (Dr. A. Ejlali)**, Hardware Implementation of a Proposed Embedded Monitor System.

2011 **Advanced microprocessors Course (Dr. A. H. Jahangir)** , Performance Analysis of Branch Prediction on State of The Art Intel Processors.

2011 **Advanced Topics in Dependable Computing Systems Course (Prof. S. G. Miremadi)** , Fault Tolerant Reconfigurable FPGAs.

2010 **Advanced Computer Architecture Course (Dr. A. H. Jahangir)** , Investigating The Software-Based Speedup Methods *and* Parallelization of Prime Number Generation Using Message Passing Interface.

2010 **Fault-Tolerant Systems Design (Prof. S.G. Miremadi)** , Investigating Fault Tolerant Features in Microcontrollers.

Languages

Farsi **Native Speaker**

English **Fluent**

Arabic **Basic**