

## Design and Simulation of a Tandem ATM Switch based on FPGA

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### **Abstract**

In this paper, design and simulation of an ATM switch based on banyan networks using Altera FLEX<sup>®</sup> 10K FPGA is reported. In the designed ATM switch, which is called tandem banyan, the problem of internal blocking is solved by providing multiple paths between each input-output pair using cascaded banyan networks. In accordance with minimum cell throughput requirement for ATM switches (about 155 Mbps), cell-processing overhead in the switch and FPGA working frequency limitation, switch architecture has been designed to work internally in the 8-bit data width. Space optimization of the AHDL code of the designed switch led to 26.45 MHz internal working frequency and a speed optimization of it, resulting in 28.9 MHz internal working speed.

**Keywords:** ATM switch, switch fabric, banyan network, tandem banyan, FPGA

### **I. Introduction**

During the last two decades communication network technology has evolved to offer the multimedia services including sound and video together with data transmission at the same time. This led to creation of ISDN and growing up to BISDN networks. ATM was introduced in mid 80's and has been selected by ITU-T as the most appropriate technique for BISDN. ATM has special protocols and layers for this purpose, high speed switching nodes and guarantees for the quality of service. ATM switches with small error rate, delay and jitter can switch ATM cells at high speeds.

FPGA technology has introduced applications in custom VLSI design and has facilitated production of integrated circuits using the prefabricated elements. Over 250,000 programmable gates in an FPGA, internal SRAM and various VHDL libraries for easy mapping of design into FPGA make the FPGA a powerful candidate for an ATM switch realization.

In the following, design and simulation of an 8-port tandem ATM switch based on ALTERA FLEX<sup>®</sup> 10K FPGA is reported. The selected architecture for the switch is a variety of banyan networks, called tandem banyan, which will be elaborated in the next section. The design and simulation of an 8x8-tandem banyan switch is presented in section III. Finally, section IV concludes the paper.

### **II. Tandem banyan switch**

Banyan networks have many useful and attractive properties, so that many complex communication switches are based on them [RaAM95].

In addition to several advantages of banyan networks such as self-routing, constant input-output delay for all I/O pairs and synchronous and asynchronous working, due to modularity and neat structure, it can be simply mapped into VLSI and scaled for larger switches with more input/outputs.

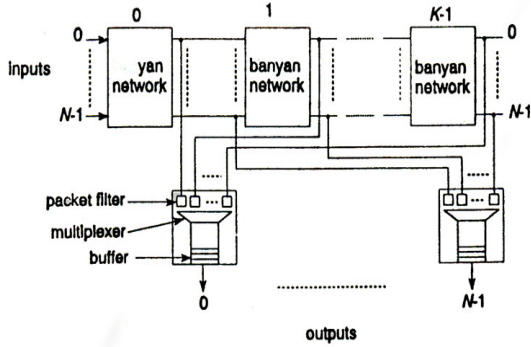
Banyan networks have two main problems that have been overcome in their extensions such as tandem banyan [Toba91].

A tandem banyan is an output-buffered switch, constructed by cascaded banyan networks (Figure.1). Providing multiple paths between each input-output

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pair, using cascaded banyan network, solves the problem of internal blocking. The blocked cells at each output stage are forwarded to the next banyan stage to be switched to the appropriate output.

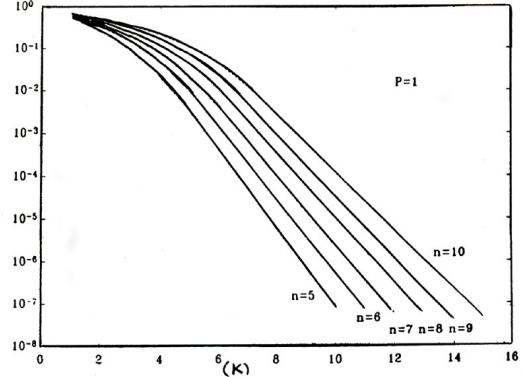


**Figure 1:** Tandem banyan switch structure [RaAM95]

Using tandem banyan modules also removes the second general problem in the banyan switches, i.e., sensitivity to input traffic pattern. In this case, special input traffic for the specific output port is regulated and switched after passing multiple stages. All the switched cells at each port of each stage are forwarded to the dedicated output queue of that port for re-sequencing. The blocked cells at the last stage may be lost or fed into the input of the last stage or the first stage. This depends on the design of the switch.

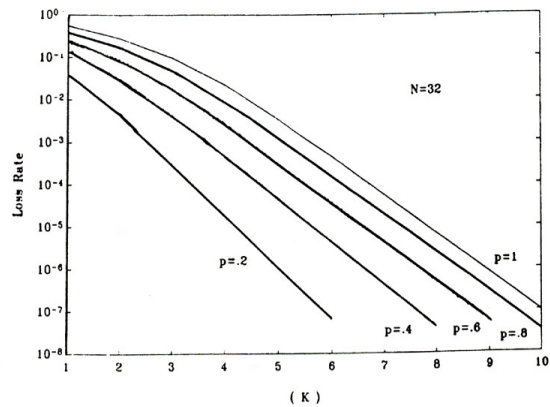
As we move through the switch stages, input load of the stage becomes lower. Therefore, selecting the proper number of stages ( $K$ ) can decrease the cell loss rate to meet the minimum cell loss rate at ATM, i.e.,  $10^{-6}$  [RoCG94]. The mathematical analysis of tandem banyan is done in the [Khan99]. As shown in Figure.2, 32 inputs ( $N=32$ ) and input probability traffic  $P=1$  using 9 stages and for  $N=1024$  using 14 stages will give the proper cell loss rate.

Heuristically, adding one stage for  $N=32$ ,  $K=5$  decreases cell loss rate about 10 times and for  $N=1024$  and  $K=9$  adding one stage decreases cell loss rate 5 times.



**Figure 2:** Cell loss rate vs. number of stages ( $K$ ) in an  $N \times N$  port, tandem banyan switch under uniform traffic

Figure.3 shows cell loss rate for various input traffic ranging from  $P=0.2$  to  $P=1$  versus number of stages for a  $32 \times 32$  switch. As the input traffic decreases, number of required stages to satisfy ATM cell loss rate is reduced. For example, under input traffic  $P=0.4$  using seven stages will give cell loss rate less than  $10^{-6}$  [Sami97]. Taking advantage of recirculation buffer at the output ports of final stage to feed the missing switched cells backed into the switch, considerably decreases the number of required stages.



**Figure 3:** Cell loss rate vs. number of stages in a  $32 \times 32$  port tandem banyan switch under different input uniform traffic

For  $N=32$ , by using only 5 stages and recirculation buffer with 4 cell depth, we can reach to ATM cell loss rate. Whereas, without recirculation buffers, we need 9 stages to obtain the proper cell loss

rate. For N=1024, using 7 stages and a recirculation buffer with 4 cell capacity at each output port, gives the suitable cell loss rate. Therefore, recirculation buffers make the switch hardware smaller.

### III. Design and Simulation

The first implementation of the tandem banyan switch as a general-purpose switch can be found in [Toba91]. This is an ASIC design using BiCMOS 0.35-micron technology with serial packet input and not adapted for ATM.

Without loss of generality, design and simulation is done for 8x8-tandem banyan switch. Regarding the FPGA internal delay and typical working speed of FPGA, the switch modules work internally in 8-bit width. Several units have been developed with AHDL<sup>1</sup>, simulated and tested with MAX+PLUS II software as briefly follows:

- **Cell processing unit:** Adds 8-bit local header at the entrance of the switch including destination port address, time stamp, and priority bit. The header fields are calculated based on the 5-byte cell header.
- **Switching element 2x2 (SE2x2):** Basic building block for constructing 8x8 banyan network
- **8x8 banyan network**
- **Input controller:** Analyzes one banyan stage output to filter the switched cells to the output buffer
- **Reorder output buffer**  
Sorts the received cells from banyan stages output based on the cells time stamps. This unit acts as a cell queue and can do simultaneous cell read and cell write. Each output port uses one such unit to handle the incoming cells from banyan stages.
- **Manager:** Generates all necessary controlling signals for other units (e.g. clock, reset...).

Among Altera FPGA families, FLEX<sup>®</sup> 10K has been selected. FLEX<sup>®</sup> 10K family has 6 kbit to 40 kbit SRAM, which is

suitable for output-buffer mapping and has up to 250,000 programmable gates [Altera98].

Pin to pin delay, working frequency and cell loss rate of the designed switch should match those of ATM standard.

Accurate simulation is done to test the functionality and timing of the circuit, and to calculate other parameters. If the internal working frequency is at least 19.4 MHz, external working frequency would be around 155 MHz. Results of timing simulation for the designed switch are presented in table 1 for the two cases of AHDL code speed and area optimizations.

Optimization method	Max. Frequency	Max. Pin to Pin Delay
Speed	28.9 MHz	19.1 ns
Area	26.45 MHz	20.2 ns

*Table 1: Maximum working frequency of the designed switch under different AHDL code optimization.*

The 4 stage 8x8 banyan network with only one reorder buffer at one port needs 7 FLEX<sup>®</sup> 10K(three 10QC208-3, two 30BC365-3, one 100GC503 and one 50bc356-3) and takes 13 hours to complete the simulation on a Pentium 233.

The simulation of cell loss rate needs an ATM traffic generator, which should implement different distributions for the cell traffic, scheduling and flow control algorithms. This testbed has been implemented [SrVa95] but was not available to us. Burst traffic, traffic source (sound, video and data) should also be considered in the cell loss rate simulation [HeTL92].

### IV. Conclusion

Lack of high-speed technology and low power consuming IC design technologies (CMOS, BiCMOS) is a motivation to implement an ATM switch using FPGA. The analysis and simulation of the designed tandem banyan switch shows the feasibility of building small ATM

<sup>1</sup> Altera Hardware Description Language

switches with FPGA. However, it requires many FPGAs and a big circuit to connect these FPGAs for the large switches. The designed switch can work at a maximum 231.2 Mbps, which is far less than that of ATM switch ASIC design with 20Gbps throughput [KaPk98].

The low speed of FPGA circuit can be overcome by designing the switch internal architecture in parallel. Distributed routing of the incoming cells, modular structure, simplicity and extendibility are some of the advantages of tandem banyan switch to fit into FPGA's. Giving acceptable throughput by using lower hardware resources and less hardware module variations versus batcher-banyan based switches [Nara88] like Starlite [HuKa84] and Sunshine [GiHi91] is another advantage for the designed switch. The designed switch is not supporting multicast or broadcast mechanisms.

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