

Power and Reliability Co-Management in Multicore Embedded Systems

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Abstract—The number and diversity of cores in embedded systems are increasing rapidly. Modern embedded processors provide multiple cores for parallel computing, and hence power dissipation and thermal issues have assumed increasing significance in embedded system design. Therefore, as the number of cores increases, power budget constraints may prevent powering all cores simultaneously at full performance level. For that reason, chip manufacturers introduce a power budget constraint as Thermal Design Power (TDP) for chips. Meanwhile, reliability has become an important concern in the design of embedded systems and multicore platforms are suitable for the implementation of fault-tolerance techniques to achieve high reliability. Thus power consumption and reliability are two main objectives in designing multicore embedded systems. In this research, we aim at considering the interactions of power and reliability management on each other in multicore embedded systems.

Index Terms—Power Consumption, Fault Tolerance, Embedded Systems, Reliability, Mapping, Scheduling.

I. INTRODUCTION

MULTICORE embedded systems, coupled with increased power consumption, pose multiple challenges such as reliability and performance. The increased power consumption in these systems leads to increased temperatures, eventually leading to a thermal violation. In order to overcome such concerns, exploiting the reliability-aware power management technique is a crucial requirement for multicore embedded systems. In [1], we have considered task replication to manage the reliability since it is a quite viable option for reliability improvement in the embedded systems with multiple processing cores and also it may tolerate permanent and transient faults. But on the other hand, careless task replication may result in a chip TDP violation. To satisfy a given reliability target and meet the TDP constraint, the level of replication and the voltage and frequency for each task should be determined cautiously. Therefore we have proposed ReMap, a peak-power-aware task replication mechanism for a set of periodic soft real-time tasks on multicore embedded systems. This method consists of three phases: the reliability-aware LU (RA-LU) Mapping, (ii) the maximum-power-aware EDF (MPA-EDF) Scheduling, and (iii) the reliability-and-peak-power-aware DVFS (RPPA-DVFS) energy management. It should be noted that due to the fact that tasks are usually completed sooner than their worst-case execution time and the correct execution of at least one of them is required for the system to be functional, successful execution of each task has taken place earlier and execution of replicas is canceled. In [2], we have introduced a two-phase peak power management (TP3M) mechanism for scheduling hard real-time

tasks in fault-tolerant multicore embedded systems. In this work, we have used passive redundancy (i.e., TMR) to tolerate both transient and permanent faults. Given that it is not feasible to simultaneously power on all cores on a multicore platform because of TDP constraint, we have proposed a scheme, that tries to remove overlaps of the peak power of concurrently executing tasks to keep the maximum power consumption below the chip TDP without violating real-time constraints. In [3], we have introduced a peak-power-aware energy management (PPA-EM) scheme that schedules main tasks on the primary core by PPA-EDF policy and backup tasks on the spare core by PPA-EDL policy in the standby-sparing system in such a way that TDP and real-time constraints are met. These policies provide the best opportunity to shift the task executions as much as possible to minimize execution overlaps between main and backup tasks that consume high power consumption. When a task finishes successfully a larger portion of its corresponding backup task can be canceled, resulting in a significant amount of peak/average power reduction. To achieve further peak/average power reduction, we use DVFS and DPM. In [4], we have proposed an RL-based DVFS method (called Ring-DVFS) to reduce power consumption without reliability degradation for sporadic tasks. The proposed method has the ability to adapt to different situations using learning capabilities to prevail over the three main concerns in the homogeneous multicore embedded systems, i.e., low power consumption, high reliability, and real-time computing. In this work, the reinforcement learner takes decisions based on the power savings and task-reliability variations due to DVFS and considers the suitable voltage-frequency level for all tasks such that the timing constraints are met.

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include low power design, real-time embedded systems, and fault-tolerant embedded systems.