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Introduction

- The largest manufacturer of SRAM-based FPGAs
- Main Families:
  - XC2000
  - XC3000
  - XC4000
  - XC5000
  - ...
## Xilinx Series Comparison

<table>
<thead>
<tr>
<th>Series</th>
<th>I/O Blocks</th>
<th>CLBs</th>
<th>FFs</th>
<th>Gate Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2000</td>
<td>58-74</td>
<td>64-100</td>
<td>122-174</td>
<td>800-1,800</td>
</tr>
<tr>
<td>XC3000</td>
<td>64-176</td>
<td>64-484</td>
<td>256-1,320</td>
<td>1,300-9,000</td>
</tr>
<tr>
<td>XC4000</td>
<td>64-256</td>
<td>64-1,024</td>
<td>256-2,569</td>
<td>1,600-25,000</td>
</tr>
<tr>
<td>XC5000</td>
<td>148-244</td>
<td>196-484</td>
<td>784-1,936</td>
<td>6000-15000</td>
</tr>
</tbody>
</table>
Xilinx FPGA Structure

- Fixed array of Configurable Logic Blocks (CLBs) connectable by a system of pass-transistors, driven by SRAM cells
XC3000 CLB

- 32-bit (5-input) look-up table
- CLB propagation delay is fixed (LUT access time) and independent of the logic function
- 7 inputs to the XC3000 CLB:
  - 5 CLB inputs (A–E)
  - 2 FF outputs (QX and QY)
XC3000 CLB Configurations

- Use 5 (of 7) inputs with the entire 32-bit LUT (CLB outputs F and G are then identical)
- Split the 32-bit LUT in half to implement 2 functions (F and G) of 4 variables each; choose 4 inputs (from 7)
- Split the 32-bit LUT in half, using one of the 7 input variables as a select input to a 2:1 MUX that switches between F and G (to implement some functions of 6 and 7 variables)
Methods of Interconnection

- Direct interconnect: Adjacent CLBs are wired together in the horizontal or vertical direction. The most efficient interconnect (< 1 ns delay)
  - General-purpose interconnect: used mainly for longer connections or for signals with a moderate fan-out
    - Few, so problem in fitting a large design into XC3000, and 2000
  - Long line interconnect: for time critical signals (e.g. clock signal need be distributed to many CLBs)

- Diagram of interconnection methods:
  - Direct Connections
  - Horizontal Long Lines
  - General Purpose Lines
  - Vertical Long Line
  - Global Long Line
Design Example

\[ Q_2^* = Q_2' Q_1 + Q_2 Q_0 \]
\[ Q_1^* = X' Q_2' Q_1' Q_0 + X' Q_2' Q_0' + X' Q_2 Q_0' + Q_1 Q_0 \]
\[ Q_0^* = Q_0' \]
\[ Z = X Q_1 + X' Q_1' \]

- Functions have maximum 4 variables
  - 4 LUT of 4 variables
  - 3 FFs
  - 2 CLB required

- FPGA Implementation
  - \( Q_2^*, Q_0^* \) in one CLB
  - \( Q_1^*, Z \) in one CLB
Design Example Implementation
## Xilinx 4000 Series

<table>
<thead>
<tr>
<th>Device</th>
<th>CLB Matrix</th>
<th>Total CLBs</th>
<th>Max. User I/O</th>
<th>Flip-Flops</th>
<th>Max. RAM bits (no logic)</th>
<th>Max. Gates (no RAM)</th>
<th>Typical Gate Range (Logic and RAM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC4002XL</td>
<td>8 x 8</td>
<td>64</td>
<td>64</td>
<td>256</td>
<td>2,048</td>
<td>1,600</td>
<td>1,000–3,000</td>
</tr>
<tr>
<td>XC4003E</td>
<td>10 x 10</td>
<td>100</td>
<td>80</td>
<td>360</td>
<td>3,200</td>
<td>3,000</td>
<td>2,000–5,000</td>
</tr>
<tr>
<td>XC4005E/XL</td>
<td>14 x 14</td>
<td>196</td>
<td>112</td>
<td>616</td>
<td>6,272</td>
<td>5,000</td>
<td>3,000–9,000</td>
</tr>
<tr>
<td>XC4006E</td>
<td>16 x 16</td>
<td>256</td>
<td>128</td>
<td>768</td>
<td>8,192</td>
<td>6,000</td>
<td>4,000–12,000</td>
</tr>
<tr>
<td>XC4008E</td>
<td>18 x 18</td>
<td>324</td>
<td>144</td>
<td>936</td>
<td>10,368</td>
<td>8,000</td>
<td>7,000–15,000</td>
</tr>
<tr>
<td>XC4010E/XL</td>
<td>20 x 20</td>
<td>400</td>
<td>160</td>
<td>1,120</td>
<td>12,800</td>
<td>10,000</td>
<td>7,000–20,000</td>
</tr>
<tr>
<td>XC4013E/XL</td>
<td>24 x 24</td>
<td>576</td>
<td>192</td>
<td>1,536</td>
<td>18,432</td>
<td>13,000</td>
<td>10,000–30,000</td>
</tr>
<tr>
<td>XC4020E/XL</td>
<td>28 x 28</td>
<td>784</td>
<td>224</td>
<td>2,016</td>
<td>25,088</td>
<td>20,000</td>
<td>13,000–40,000</td>
</tr>
<tr>
<td>XC4025E</td>
<td>32 x 32</td>
<td>1,024</td>
<td>256</td>
<td>2,560</td>
<td>32,768</td>
<td>25,000</td>
<td>15,000–45,000</td>
</tr>
<tr>
<td>XC4028E/XL</td>
<td>32 x 32</td>
<td>1,024</td>
<td>256</td>
<td>2,560</td>
<td>32,768</td>
<td>28,000</td>
<td>18,000–50,000</td>
</tr>
<tr>
<td>XC4036E/XL</td>
<td>36 x 36</td>
<td>1,296</td>
<td>288</td>
<td>3,168</td>
<td>41,472</td>
<td>36,000</td>
<td>22,000–65,000</td>
</tr>
<tr>
<td>XC4044XL</td>
<td>40 x 40</td>
<td>1,600</td>
<td>320</td>
<td>3,840</td>
<td>51,200</td>
<td>44,000</td>
<td>27,000–80,000</td>
</tr>
<tr>
<td>XC4052XL</td>
<td>44 x 44</td>
<td>1,936</td>
<td>352</td>
<td>4,576</td>
<td>61,952</td>
<td>52,000</td>
<td>33,000–100,000</td>
</tr>
<tr>
<td>XC4062XL</td>
<td>48 x 48</td>
<td>2,304</td>
<td>384</td>
<td>5,376</td>
<td>73,728</td>
<td>62,000</td>
<td>40,000–150,000</td>
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<tr>
<td>XC4085XL</td>
<td>56 x 56</td>
<td>3,136</td>
<td>448</td>
<td>7,168</td>
<td>100,352</td>
<td>85,000</td>
<td>55,000–180,000</td>
</tr>
</tbody>
</table>
Xilinx 4000 Specs

- Two FF per CLB + Two per I/O cell
- 25 gates per CLB for logic
- 32 bits of RAM per CLB
- Special fast carry logic between CLBs
- Interconnects:
  - Direct and general-purpose wires replaced with more efficient single-length and double-length lines.
  - Sufficient resources for most applications.
Xilinx 4000 CLB
CLB Function Generators

- Use RAM for truth tables
  - F, G: 4 input -> 16 bits of RAM (each)
  - H: 3 input -> 8 bits of RAM
  - RAM is loaded at system initialization from external PROM

- MUX control logic maps 4 control inputs into 4 inputs:
  - LUT input H1
  - Direct In (DIN)
  - Enable Clock (EC)
  - Set/Reset control (S/R) for FFs
  - Control F,G LUTs as 32 bit SRAM
CLB Function Generators (cont.)

- **Broad capability:**
  - Any 2 functions of 4 variables plus a function of 3 variables
  - Any function of 5 variables
  - Any function of 4 variables plus some functions of 6 variables
  - Some functions of 9 variables
    - Parity
    - 4-bit cascadable equality checking
CLB input and output connections
Programmable Switch Matrix

programmable switch element

turning the corner, etc.
XC5200 Logic Block

- Similar to CLBs in XC2000/3000/4000, but simpler
- A group of 4 Logic Cells (LCs) is a CLB in XC5200
- LC contains 4-input LUT
State-of-the-art FPGAs

- **XCS00/XL (Spartan)**
  - 5v, 3v
  - 2,000-40,000 typical gate

- **XC2S00/XL (Spartan-II)**
  - 2.5v
  - 6,000-150,000 typical gate

- **XCV00 (Virtex)**
  - 2.5v
  - 34,000-1,124,000 typical gate
State-of-the-art FPGAs (cont.)

- **1999**: Virtex-E
- **2000**: Virtex-II
- **2002**: Virtex-II Pro
  - 125,136 logic cell
  - 10 Mb RAM
  - 556 18*18 Multiplier
  - Up to 4 PowerPC 405 cores
    - 300 MHz+, 420 MIPS