VLSI Design
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Description and Aim:
Comprehensive understanding of the CMOS VLSI design concepts, including CMOS processing technology, CMOS static and dynamic logic, performance estimation and optimization in both layout- and logic-levels, as well as concerns related to combinational, sequential, interconnect, and datapath systems are extremely important for today’s digital designers. This course is syllabused to address most of these issues through lecture, projects, theoretical, and computer assignments. The course will give insight on how to get from a layout, circuit, logic, and system level descriptions to an efficient VLSI implementation using various architectural techniques while considering a given set of criteria. In fact, the course provides a practical understanding of the implementation strategies for digital ICs, existing VLSI technologies, fundamentals of digital logic design, common combinational, sequential, interconnect, and datapath design techniques, as well as VLSI techniques for high-speed/low-power designs. State-of-the-art design tools will be used to support the course work. As a part of the course requirement is a term project on the design and implementation of a digital sub-system, which is assigned in the middle of the semester and will be completed in parallel to the lectures.

Tools:
+ Synoptic DC/PC, HSPICE, LEDIT, SOCE

Course Composition:
+ Assignment {theoretical and computer}, Quizzes, Midterms, Final Project, Final Exam
+ VLSI Design course page at CE: Calendar + Grading policy

References:

Prerequisites:
+ Verilog/VHDL, Circuit-level design based on HSPICE, Digital electronic.
Syllables

1- Digital Systems and VLSI \{Wolf + Weste + Rabaey\}
   a. Why Design Integrated Circuits?
   b. Integrated Circuit Manufacturing
   c. CMOS Technology
   d. Integrated Circuit Design Techniques
   e. IP-Based Design

2- Fabrication Process: CMOS Processing Technology \{Wolf + Weste\}
   a. Fabrication Processes
      i. Design Rule Background
      ii. Scribe Line and Other Structures
      iii. MOSIS Scalable CMOS Design Rules
      iv. Micron Design Rules
      v. CMOS Process Enhancements: Performance, Power, Yield
   b. Transistors
   c. Wires and Vias
   d. Fabrication Theory and Practice
   e. Reliability
   f. Layout Design and Tools

3- MOS Transistor Theory \{Wolf + Rabaey\}
   a. Detailed I-V and C-V Characteristics
   b. Detailed MOS Capacitance Model
   c. Non-ideal IV-Effect
   d. DC Transfer Characteristics

4- Logic Gates \{DeMassa + Weste + Rabaey\}
   a. Introduction
   b. Combinational Logic Functions
   c. Static Complementary Gates
   d. Switch Logic
   e. Alternative Gate Circuits
   f. Low-Power Gates
   g. Delay through Resistive Interconnect
   h. Delay through Inductive Interconnect
   i. Design-for-Yield

5- Combinational Circuit Design \{DeMassa + Weste\}
   a. Circuit Families
b. Circuit Pitfalls

c. More Circuit Families

d. Silicon-On-Insulator Circuit Design

e. Subthreshold Circuit Design

6- Sequential Circuit Design \{DeMassa + Weste\}

a. Sequencing Static Circuits
b. Circuit Design of Latches and Flip-Flops
c. Static Sequencing Element Methodology
d. Sequencing Dynamic Circuits
e. Synchronizers
f. Wave Pipelining

7- Delay Estimation and Optimization \{Weste\}

a. RC Delay Model
b. Elmore Delay Model
c. Layout Dependence of Capacitance
d. Linear Delay Model
e. Logical Effort
f. Logical Effort of Paths
g. Delay in Multistage Logic Networks
h. Choosing the Best Number of Stages
i. Limitations of Logical Effort
j. Timing Analysis Delay Models

8- Power Estimation and Optimization \{Weste\}

a. Sources of Power Dissipation
b. Dynamic Power
c. Static Power
d. Energy-Delay Optimization
e. Low Power Architectures

9- Subsystem Design \{Wolf + Weste\}

a. Datapath Subsystems
   i. Addition/Subtraction
   ii. One/Zero Detectors
   iii. Comparators
   iv. Counters
   v. Boolean Logical Operations
   vi. Coding
   vii. Shifters
      1. Funnel Shifter
2. Barrel Shifter
3. Alternative Shift Functions
   viii. Multiplication
   ix. Parallel-Prefix Computations
b. Array Subsystems
   i. SRAM
   ii. DRAM
   iii. Read-Only Memory
   iv. Serial Access Memories
   v. Content-Addressable Memory
   vi. Programmable Logic Arrays
   vii. Robust Memory Design
       1. Redundancy
       2. Error Correcting Codes (ECC)

10- Floorplanning \{Wolf\}
   a. Floorplanning Methods
   b. Global Interconnect
   c. Floorplan Design
   d. Off-Chip Connections