The Agilent Technologies 16557D 140MHz State/500MHz Timing Logic Analyzer at 140 MHz has the fastest state speed available with 2M-deep memory.*

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* In a five-card module, the state speed is 100 MHz.
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Agilent Technologies 16557D 140MHz State/500MHz Timing Logic Analyzer
Setting Up a Measurement

After you have connected the logic analyzer probes to your target system, (see page 10) there are five basic steps for any measurement.

1. “Define the Type of Measurement” on page 11
2. “Set Up the Bus Labels” on page 13
3. “Define Trigger Conditions” on page 14
4. “Run the Measurement” on page 15
5. “Examine the Data” on page 16

Refine measurement by repeating steps 3 - 5.

If you load a configuration file, it will set up the logic analyzer and trigger. For your particular measurement, you may need to change some settings.

See Also

“Making a Basic Timing Measurement” on page 22
“Making a Basic State Measurement” on page 18
Measurement Examples (see the Measurement Examples help volume)
Making Basic Measurements for a self-paced tutorial

Connect the Analyzer to the Target System

Before you begin setting up a measurement, you need to physically connect the logic analyzer to your target system. Attach the pods in a way that keeps logically related channels together and be sure to...
Setting Up a Measurement

ground each pod. *Analysis probes*, available for most common microprocessors, can simplify the connection process.

The logic analyzer pods carry the signals to the logic analyzer from your target system. Connect the pods either directly to the target system or to an analysis probe. You can attach the pods either directly to a 40-pin header, to a 20-pin header with an adapter, or use the General Purpose Probes to attach to individual channels.

If you are using an analysis probe, Setup Assistant will guide you through the process based on your logic analyzer and the analysis probe.

Step 1: Describe the Measurement (see page 11)

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**See Also**

“Analyzer Probing Overview” on page 92 for more detail on types of probes

Setup Assistant (see the *Setup Assistant* help volume)


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Define the Type of Measurement

There are two types of measurements: *state measurements* and *timing measurements*. Use the *Sampling* tab to select either type and to specify the details particular to that type.
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Setting Up a Measurement

Choose State or Timing

In a state measurement, the analyzer uses an external clock to determine when to sample. Each time the analyzer receives a state clock pulse, it samples and stores the logic state of the target system.

In a timing measurement, the analyzer is analogous to an oscilloscope. It samples at regular time intervals and displays the information in a waveform similar to the oscilloscope.

Set Measurement Mode

Each measurement type has different measurement modes. In general, there is a trade-off between number of signals and speed.

Because the measurement type and mode affect clocking and trigger options, you must set the measurement type first.

Set up State Clock

For state measurements, you must specify a clock to match the clocking arrangement used by your target system. It can be as simple as a single rising edge, or a complex arrangement of up to four signals. If the clock is incorrect, the trace data may indicate a problem where there isn’t one. Specify the state clock in Clock Setup.

The equivalent in timing mode of the state clock is the Sample Period. The Sample Period sets the time between logic analyzer samples. For reliable data, the sample period should be no more than half of your clock period. Many engineers prefer setting it to one-fourth of the clock period.

Set up the Trace

The remaining controls finish your description of how you want to capture data. The trigger position determines where the events you specify in the trigger sequence will be relative to the majority of the data the logic analyzer captures.

Memory depth is affected by the measurement mode. Some logic analyzers also let you limit how big the acquisition will be with an Acquisition Depth control.

Step 2: Set Up the Bus Labels (see page 13)
Chapter 1: Agilent Technologies 16557D 140MHz State/500MHz Timing Logic Analyzer

Setting Up a Measurement

See Also

“The Sampling Tab” on page 41 for information on setting type and assigning pods

“Setting the Acquisition Mode” on page 42 for links to this analyzer’s modes

“Performing Clock Setup (State only)” on page 42

Set Up the Bus Labels

The next step is to finish defining the physical connection between the target system and the analyzer. Use the Format tab to tell the analyzer what you want to measure on the target system. If you load a configuration file, this step is taken care of for you.

Group and Label Signals

Because the logic analyzer can capture dozens or even hundreds of signals, you need to organize the signals by grouping and labeling channels. Labels are used to group these channels into logical signals; for example, "addr bus". These groupings are then used in the trigger tab and the data displays. A label can have up to 32 channels. Each measurement can define 126 labels. Active channels are indicated like so.

Set Threshold Level

The logic analyzer needs to know what threshold level the target system is using. You can set the analyzer to use TTL or ECL logic levels,
or set a different threshold voltage. The logic analyzer requires a minimum voltage swing of 500 mV at the probe tip to recognize changes in logic levels.

Step 3: Define Trigger Conditions (see page 14)

**See Also**

“Assigning Bits to a Label” on page 51

“The Format Tab” on page 49

**Define Trigger Conditions**

The third step is to define the trigger. The trigger settings tell the analyzer when you want to capture data. Controls for this are located under the *Trigger* tab. Configuration files saved from previous measurements automatically define trigger settings.

**Set Up a Trigger Sequence**

The trigger sequence is like a small program that controls when the logic analyzer stores data. There are trigger functions for the common tasks, or you can set up your own. The logic analyzer starts at the first trigger level, and stays there until the conditions described in that level become true. When that happens, the logic analyzer goes to the next level and follows the instructions there.
Define Terms

Trigger terms are like variables that you use in the trigger sequence. Depending on what analyzer you are using, you can either assign the values directly from within the trigger sequence or from the tabs (pattern, range, edge).

Step 4: Run the Measurement (see page 15)

See Also

“Defining Resource Terms” on page 79
“Understanding Logic Analyzer Triggering” on page 61
“Setting Up a Trigger” on page 63
“The Trigger Tab” on page 60
Measurement Examples (see the Measurement Examples help volume)

Run the Measurement

You run the measurement by selecting the Run button. The Run button is labeled either Run, Group Run, or Run All. The difference between the three types is that Run starts only the instrument you are using, Group Run starts all instruments attached to group run in the Intermodule window, and Run All starts all instruments currently placed in the workspace.
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Setting Up a Measurement

Select Single or Repetitive
Risks can be single or repetitive. Single runs gather data until the logic analyzer memory is full, and then stop. Repetitive runs keep repeating the same measurement and are useful for gathering statistics. To stop a run, select the Stop button.

NOTE:
Repetitive runs on a logic analyzer don’t do equivalent time sampling like oscilloscopes do.

If Nothing Happens...
Analyzers with deep memory take a noticeable amount of time to complete a run. Because data is not displayed until acquisition completes, it may look like nothing is happening. Check the Run Status window to see if the logic analyzer is still running. Messages such as "Waiting in level 1" may indicate you need to refine your trigger. If the status shows as "Stopped", the analyzer either finished the acquisition, or was unable to run. The cause of the problem is listed in the bottom half of the Run Status window, and the messages are explained in more detail in “Error Messages” on page 33.

Step 5: Examine the Data (see page 16)

See Also
“When Something Goes Wrong” on page 33

Examine the Data

Data from your measurement can be viewed in various display windows or offline. Some of the things you can do in the display windows are
• Search for patterns
• Display time-correlated data
• Use markers to make measurements and gather statistics

Search for Patterns

You can search displays for certain values, and place markers on them. There are two global markers which keep their place across all measurement views, even across instruments.

Display Correlated Data

There are several tools for correlation. The Intermodule window allows you to specify complex triggering configurations using several instruments. It is also useful for starting acquisitions at the same time. Global markers mark the same events in different displays, so you can switch views without having to reorient yourself. The Compare tool lets you compare two different acquisitions to look for changes.

Use Markers to Make Measurements

The markers can be positioned relative to the beginning, end, trigger, or another marker, as well as set to a specific pattern, state, or time. The Markers tab in the Display windows shows the time or state value as you move the markers or take new acquisitions.

See Also

- Working with Markers (see the Markers help volume)
- Using the Chart Display Tool (see the Chart Display Tool help volume)
- Using the Distribution Display Tool (see the Distribution Display Tool help volume)
- Using the Listing Display Tool (see the Listing Display Tool help volume)
- Using the Digital Waveform Display Tool (see the Waveform Display Tool help volume)
- Using the Compare Analysis Tool (see the Compare Tool help volume)
- “Interpreting the Data” on page 26
Making a Basic State Measurement

This example uses the circuit board that is supplied with the *Making Basic Measurements* kit as the target system. The kit is supplied with every logic analysis system, or can be ordered from your Agilent Technologies Sales Office.

There are six major steps to making a basic measurement.

1. Connect probes.
   - Connect Pod 1 of the logic analyzer to J1 on the target system.

   The training board has terminations and headers already built in to the system, so you can connect the logic analyzer pod directly to the board.

2. Define the type of measurement On the Agilent Technologies 16700A/B logic analysis system, open a logic analyzer setup window.
   a. In the main window, select the logic analyzer icon.
   b. Choose *Setup...* from the menu.
   c. Select the *Sampling* tab.
   d. If the logic analyzer is not already set for *State*, change the type to *State*.

3. Set up the clock to match the target system's clocking scheme.
   a. In the bottom half of the *Sampling* tab window, choose the correct edges to match your clock. For Pod 1 attached to the training board, the correct clock is the falling edge on J.
      1. Select the *Off* button under J and choose "Falling Edge" from the menu.

4. Group and label bits.
   a. Select the *Format* tab.
   b. Optional - Insert a second label.
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Making a Basic State Measurement

1. Select the Label1 button.

2. Choose Insert after...

3. In the Enter Label Name box, select the OK button.

c. Optional - Rename Label1.

1. Select the Label1 button.

2. Choose Rename....

3. Enter a new name in the name field.

4. Select the OK button to close the Rename Label box.

d. Select the bit assignment button.

The bit assignment button is to the right of a label name, and under a pod column.

e. Choose ........******** from the menu.

If none of the choices match your own system, choose Individual...

and select the individual bits to assign them (*) or ignore them (.)

5. Define trigger events for patterns on buses.

a. Select the Pattern subtab in the Trigger tab.

b. Optional - Rename Pattern1.

1. Select the Pattern1 field.

2. Enter a new name.

c. Select the appropriate label.

1. Select the label name button.

2. To define the event as a combination of labels, choose Insert... To use a different label to define the event, choose Replace...

3. In the dialog box, select the label name you want to use and then select the OK button.

d. Select the field with XX and enter the value you want to trigger on.

e. Optional - Repeat steps a - d for Pattern2.

6. Optional - Add additional trigger events to the trigger specification.
Making a Basic State Measurement

The logic analyzer automatically triggers on Pattern1, the first trigger event. You can set up more complex triggers by editing the sequence levels and combining trigger events.

a. Select the sequence level number 1 button and choose Edit...

b. In the dialog box, select the Pattern1 button just after Trigger on and choose Combo...

c. In the Combination box, select the Off option button next to Pattern2 and choose On.

d. To change the trigger to Pattern1 and Pattern2, select the Or option button to the right of the events and choose And.

e. Select the OK button.

f. Select the Close button.

The analyzer is now set to trigger when it detects both the pattern defined by Pattern1 and the pattern defined by Pattern2 on the target system’s buses. The trigger sequence windows shows

```
Trigger on "(Pattern1.Pattern2)" 1 time
```

See Also

1. Select the Run button.

2. Examine the data.

   a. Select the Window menu.

   b. Select Analyzer<A> in the menu and choose Listing<1>.

       Depending on what other instruments are active, there may be more than one Analyzer<A>. Choose the one that refers to your analyzer.

   c. To have the listing display appear automatically when you run the logic analyzer, select Options -> Popup on Run -> On in the menu bar of the listing display.

   d. To insert additional labels, select the label name.

See Also

For Connection Information

"Logic Analysis System and Measurement Modules Installation Guide"
Making a Basic State Measurement

For Details on the Training Board or More Tutorials

Making Basic Measurements

Examples of Typical Timing Measurements

The "Looking at State Events" group under Hardware Turn-On (see the Measurement Examples help volume) measurements.

Firmware Development (see the Measurement Examples help volume) measurements.

System Integration (see the Measurement Examples help volume) measurements.

For Details on the Logic Analyzer Interface

“The Sampling Tab” on page 41

“The Format Tab” on page 49

“The Trigger Tab” on page 60
Making a Basic Timing Measurement

This example uses the circuit board that is supplied with the Making Basic Measurements kit as the target system. The kit is supplied with every logic analysis system, or can be ordered from your Agilent Technologies Sales Office.

There are six major steps to making a basic measurement.

1. Connect probes.
   - Connect Pod 1 of the logic analyzer to J1 on the target system.

   The training board has terminations and headers already built in to the system, so you can connect the logic analyzer pod directly to the board.

2. Define the type of measurement. On the Agilent Technologies 16700A/B logic analysis system, open a logic analyzer setup window.
   a. In the main window, select the logic analyzer icon.
   b. Choose Setup... from the menu.
   c. Select the Sampling tab.
   d. If the logic analyzer is not already set for Timing, change the type to Timing.

3. Group and label bits.
   a. Select the Format tab.
   b. Optional - Insert a second label.
      1. Select the Label1 button.
      2. Choose Insert after...
      3. In the Enter Label Name box, select the OK button.
   c. Optional - Rename Label1
      1. Select the Label1 button.
2. Choose Rename…

3. Enter a new name in the name field.

4. Select the OK button to close the Rename Label box.

d. Select the bit assignment button.
   The bit assignment button is to the right of a label name, and under a pod column.

e. Choose ...........******** from the menu.
   If none of the choices match your own system, choose Individual...
   and select the individual bits to assign them (*) or ignore them (.).

4. Define trigger events for a bus.
   a. Select the Trigger tab.
   b. Select the Pattern subtab.
   c. Optional - Rename pattern Pattern1.
      1. Select the Pattern1 field.
      2. Enter a new name.
   d. Select the appropriate label.
      1. Select the label name button.
      2. To define the event as a combination of labels, choose Insert... To use a different label to define the event, choose Replace...
      3. In the dialog box, select the label name you want to use and then select the OK button.
   e. Select the field with XX and enter the value you want to trigger on.

5. Define trigger events for an edge.
   a. Select the Edge subtab.
   b. Optional - Rename Edge1.
      1. Select the Edge1 field.
      2. Enter a new name.
   c. Select the appropriate label.
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Making a Basic Timing Measurement

1. Select the label name button.

2. To define the event as a combination of labels, choose Insert... To use a different label to define the event, choose Replace... Edges within an event are always OR’d together, which means only one of the edges on one of the labels needs to occur for the edge event to become true.

3. In the dialog box, select the label name you want to use and then select the OK button.

   d. Select the edge assignment button (........) and enter the edge or edges you want to trigger on. Remember, if more than one edge is specified, then when the logic analyzer detects any of the edges the event becomes true.

6. Add the edge event to the trigger specification.

   a. Select the sequence level number 1 button and choose Edit...

   b. In the dialog box, select the Pattern1 button and choose Combo...

   c. In the Combination box, select the Off option button next to Edge1 and choose On.

   d. Select the Or option button where the path from Pattern1 and the path from Edge1 come together, and choose And.

   e. Select the OK button.

   The analyzer is now set to trigger when it detects Edge1 and Pattern1 on the bus. The trigger sequence window shows

   Trigger on Pattern1.Edge1 occurs 1 times

   The logic analyzer automatically triggers on the first trigger event. You can set up more complex triggers by editing the sequence levels and defining additional trigger events.

See Also

“The Trigger Tab” on page 60

1. Select the Run button.

2. Examine the data.

   a. Select the Window menu.
b. Select \texttt{Analyzer\textless A\textgreater} in the menu and choose \texttt{Waveform\textless 1\textgreater}. Depending on what other instruments are active, there may be more than one \texttt{Analyzer\textless A\textgreater}. Choose the one that refers to your analyzer.

c. To have the waveform display appear automatically when you run the logic analyzer, select Options -> Popup on Run -> On in the menu bar of the waveform display.

d. To insert additional labels, or expand overlaid signals, select the label name.

\textbf{See Also}

For Connection Information

\textit{Logic Analysis System and Measurement Modules Installation Guide}

For Details on the Training Board or More Tutorials

\textit{Making Basic Measurements}

\textbf{Examples of Typical Timing Measurements}

Hardware Turn-On (see the \textit{Measurement Examples} help volume) measurements.

Firmware Development (see the \textit{Measurement Examples} help volume) measurements.

System Integration (see the \textit{Measurement Examples} help volume) measurements.

\textbf{For Details on the Logic Analyzer Interface}

“The Sampling Tab” on page 41

“The Format Tab” on page 49

“The Trigger Tab” on page 60
Interpreting the Data

After you’ve acquired a trace with the logic analyzer, you can analyze it in the display tools. The logic analysis system also provides filtering and compare tools for more complex analysis.

The logic analyzer is automatically connected to the Waveform and Listing displays when you set up a measurement. To move to that display,

1. Select the Window menu.
2. Select the name of the analyzer whose data you want to view.
3. Choose Waveform or Listing.
   Source Viewer brings up a Listing display but requires an inverse assembler and an ADDR label.
   - “Analysis Using Waveform” on page 26
   - “Analysis Using Listing” on page 28

Analysis Using Waveform

Waveform is most useful for timing data. If you look at state data that uses store qualification, you won’t be able to easily see where samples were not stored. Timing data, however, is periodic and stores all samples and so works well with Waveform.

Example: Looking for a Missing Pattern

You can easily use the waveform tool to make timing measurements. For example, if you were triggering when a pattern doesn’t follow an edge within a certain time (see the Measurement Examples help volume), you would probably want to look at your data set to see if the pattern ever did occur. This might be the case when you verifying that the system is responding to an interrupt.

After triggering on an instance where the response did not appear quickly enough, you might take these steps in the Waveform display:
1. Find the edge.
   a. Select the *Search* tab.
   b. Select the down arrow after the Label field, and select the label containing the edge.
   c. Select the Value field and enter 1.
   d. Select the *Next* button to locate the edge transition.

2. Place a marker on the edge.
   Select the *Set G1* button. This sets global marker G1 at the location of the edge you just found.

3. Search for the pattern. Searches start at your current location. Since you just set the global marker G1, it indicates where the search starts from.
   a. Select the down arrow after the Label field, and select the label containing the pattern.
   b. Select the Value field and enter the pattern you are searching for.
   c. Select the down arrow after the When field and select *Entering*.
   d. Select the *Next* button to find the next occurrence of that pattern after G1.

   If the logic analysis system cannot find the pattern, a "Value not found" message pops up.

4. Place a marker on the pattern.
   Select the *Set G2* button. This will set global marker G2 at the location of the pattern.

5. Find the time between the edge and the pattern.
   a. Select the *Markers* tab.
   b. In the G2 row, select the down arrow after from, and select G1.

   The value after the from field changes to the time between G1 and G2. You can toggle between time and samples by selecting the arrow after the Time or Samples field.

**See Also**

Using the Digital Waveform Display Tool (see the *Waveform Display Tool*
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Interpreting the Data

help volume)

Using the Listing Display Tool (see the Listing Display Tool help volume)
Using the Chart Display Tool (see the Chart Display Tool help volume)
Using the Distribution Display Tool (see the Distribution Display Tool help volume)
Using the Compare Analysis Tool (see the Compare Tool help volume)
Using the Pattern Filter Analysis Tool (see the Pattern Filter Tool help volume)

Analysis Using Listing

Listing is more useful than Waveform when your target system is running code because it shows the labels as states rather than transitions. Listing is especially useful when you have defined meaningful symbol names for your states. If you have an inverse assembler, you might prefer Source Viewer which functions like Listing.

Example: Examining a Subroutine

Listing is the preferred display tool for state measurements. for example, if you were trying to see if a subroutine were exiting abnormally, you might want to measure the number of states between entering and exiting the subroutine. After acquiring data with the logic analyzer, you could examine the data set in the Listing display like this:

1. Find the start of the subroutine.
   Assume the subroutine starts at the address 0x58FC.
   a. Select the Search tab.
   b. Select the down arrow after the Label field, and select ADDR.
   c. Select the Value field, and enter the starting address, 0x58FC.
   d. Select the down arrow after the When field and select Present.
   e. Select the Next or Prev button to move the display to the address.
2. Place a marker on the start of the subroutine.
   Select the Set G1 button. This sets global marker G1 at the address you just found.

3. Find the end of the subroutine.
   Assume the end of the subroutine is at address 0x58FF. Searches always start at the current location. Since you just set the global marker G1, it indicates where the search starts from.
   a. Select the Value field, and enter 58FF.
   b. Select the Next button to find the next occurrence of 0x58FF after the starting address.

4. Place a marker on the end of the subroutine.
   Select the Set G2 button to set global marker G2 at this position. This lets you refer to G2 when you want to know where the subroutine ends.

5. Find the number of states between the start and end of the subroutine.
   Since you’ve placed markers at the start and end of the subroutine, all you have to do is find the number of states between those markers.
   a. Select the Markers tab.
   b. In the G2 row, select the second down arrow and select Sample.
   c. Select the down arrow after from, and select G1.
   The value after the from field changes to the number of states between G1 and G2. You can toggle between time and states by selecting the arrow after the Time or Samples field.

Now you know how long the execution stayed in the subroutine, and can also examine the data set between G1 and G2 to look for unusual data.

See Also

Using the Digital Waveform Display Tool (see the Waveform Display Tool help volume)
Using the Listing Display Tool (see the Listing Display Tool help volume)
Using the Chart Display Tool (see the Chart Display Tool help volume)
Using the Distribution Display Tool (see the Distribution Display Tool help volume)
Interpreting the Data

Using the Compare Analysis Tool (see the Compare Tool help volume)

Using the Pattern Filter Analysis Tool (see the Pattern Filter Tool help volume)
Coordinating Measurements

When you want to coordinate the triggering of two measurements happening on the same logic analyzer, you need to use arming control. The two measurement machines are by default controlled by the same run button. However, you can set machine 1 to arm machine 2, or the other way around.

If the timing measurement and state measurement are being handled by two different instruments, you can coordinate them by connecting both instruments to the same display, and then setting the correlation in the correlation dialog that appears.

You can tell which instrument is controlling a measurement by looking at the instrument icon. The letter on the icon represents the slot of the frame that the instrument is in. Icons with the same letter are controlled by the same instrument.

See Also

Overview - Multiple Instrument Configuration (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)

Overview - Multiple Machine Configuration (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)
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Loading and Saving Logic Analyzer Configurations

The Agilent Technologies 16557D logic analyzer settings and data can be saved to a configuration file. You can also save any tools connected to the logic analyzer. Later, you can restore your data and settings by loading the configuration file into the logic analyzer.

The Agilent Technologies 16557D logic analyzer can also load configuration files generated for Agilent Technologies 16550A, 16554A, 16555A, 16555D, 16556A, and 16556D models of logic analyzer. However, the data cannot be displayed across logic analyzer models, and some settings may change when no comparable setting exists in the Agilent Technologies 16557D logic analyzer.

NOTE: The Agilent Technologies 16700A/B-series logic analysis systems can translate configuration files from Agilent Technologies 16500 and 16505A logic analysis systems if the measurement module is the same. If the modules are different, first load the configuration file into a module of the same type on the new logic analysis system. Re-save the configuration, then load this configuration into the destination module on the new system.

See Also

Loading Configuration Files (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)

Saving Configuration Files (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)
When Something Goes Wrong

- “Nothing Happens” on page 39
- “Error Messages” on page 33
- “Suspicious Data” on page 39
- “Interference with Target System” on page 33

Interference with Target System

Excessive capacitive loading can degrade signals, resulting in suspicious data or even system lockup. All analysis probes add capacitive loading, as can custom probes you design for your target. To reduce loading, remove as many pin protectors, extenders, and adapters as possible.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems running at frequencies greater than 50 MHz.

Error Messages

- “Slow or Missing Clock” on page 34
- “Waiting for Trigger” on page 37
- “Timer is Off in Sequence Level Where It Is Used” on page 36
- “Timer is Specified in Sequence, But Never Started” on page 35
- “Measurement Initialization Error” on page 34
- “Two Pod Pairs are Needed To Use Both Timers” on page 37
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When Something Goes Wrong

“Incompatible Time Tags Not Loaded” on page 38
“Incompatible Data Not Loaded” on page 38
“Incompatible Timing Data Not Loaded” on page 38
“Cannot Read Unrecognized Data” on page 38
“Tag Data Has Been Discarded” on page 38
“Measurement Error: Check Probe Parametrics or Grounding” on page 38

Maximum of 32 Channels Per Label

The logic analyzer can only assign up to 32 channels for each label. If you need more than 32 channels, assign them to two labels and use the labels in conjunction.

See “Adding and Deleting Labels for Terms” on page 85 for how to use more than one label with trigger terms.

Measurement Initialization Error

The logic analyzer module failed the internal calibration which it performs when Run is selected. An internal calibration failure can indicate either a software or a hardware problem.

Possible Causes

- Hardware failure
- Software failure

Run the Self-Test Utility (see page 40) on the logic analyzer and contact your Agilent Technologies Sales Office for service or software upgrades.

Slow or Missing Clock

The message "Slow or Missing Clock" only appears in state measurements. However, if you have another instrument armed by the state analyzer, a slow or missing clock on the state analyzer will prevent the other instrument from triggering also.
Possible Causes

- Target system is not running properly
  Check that the system is running properly. The logic analyzer and other probing fixtures such as pin extenders can place too much capacitive load on a system.

- Incorrect clock specification
  Make sure the target system clock matches the clock specified under Sampling. Also check that the probe's clock channels are attached to the target's clock lines either directly or through an analysis probe. If you are using an analysis probe, the probe's User's Guide should show the correct connections and settings.

- Bad probe connection
  Check that the probe is securely attached to the clock line and is receiving a signal. The logic analyzer shows activity indicators under the Sampling and Format tabs.

- Incorrect signal level
  The clock's threshold level is set by the pod threshold. For the logic analyzer's J clock, check the pod threshold of pod 1 of the master card.

See Also

“Performing Clock Setup (State only)” on page 42
“Setting the Pod Threshold” on page 57

Timer is Specified in Sequence, But Never Started

This error occurs because you have used a timer term in your trigger sequence, but not turned the timer on using the timer controls. Timer controls are available in all sequence levels except the first. You do not need to turn on the timer in the same sequence level, but it does need to be on when it is used in the trigger sequence.

This error message always occurs with the Timer is off in sequence level where it is used warning.
See “Using Timer Terms” on page 83 for more information on timer control.

**Timer is Off in Sequence Level Where It Is Used**

Timer controls are available in all sequence levels except the first. You do not need to turn on the timer in the same sequence level, but it does need to be on when it is used in the trigger specification.

**Possible Causes**

This warning occurs because you have used a *timer term* in your *trigger specification*, but not turned the timer on using the timer controls.

This warning message always occurs with the

*Timer is specified in sequence, but never started* error message.

See “Using Timer Terms” on page 83 for more information on timer control.

**Trigger inhibited during timing prestore**

The “trigger inhibited” informational message appears when you have a logic analyzer making a *timing measurement*, and it is set to a slow sample rate. The logic analyzer will fill the designated amount of pre-trigger memory before checking for the trigger condition.

To calculate how long this should take, multiply the sample rate by the percentage of pre-trigger memory and the acquisition depth. For example, if

- sample period = 1.0 ms (sample rate = \(10^3\) samples/sec.)
- trigger position = center (percentage of pre-trigger memory = 50%)
- acquisition depth = 64K (roughly \(64 \times 10^3\) samples)

then the approximate time is 32 seconds.
Two Pod Pairs are Needed To Use Both Timers

Possible Causes

This message only occurs when all pod pairs are assigned, and the machine which is using both timers has only one pod pair.

You can either assign another pod pair to the machine with both timers, or change your trigger specification to use only one timer term.

See Also

“Using Timer Terms” on page 83

Waiting for Trigger

This message indicates that the specified trigger pattern has not occurred. This may be expected, as when you are waiting to trigger on an unusual event.

Possible Causes

- Misaligned boundaries for addresses
  
  When the target is a microprocessor that fetches only from long-word aligned addresses, if the trigger is set to look for an opcode fetch at an address that is not properly aligned, the trigger will never be found.

- Trigger set incorrectly

Some strategies you can use when verifying or debugging trigger sequence levels are:

- Look at the run status message line or open the Run Status window. It will tell you what level of the sequence the logic analyzer is in.

- Stop the measurement and look at the data that was captured. This is particularly useful when you use store qualifiers to store "no states" (or only the states you are interested in) and the branches taken are stored.

- Save the trigger setup, then simplify it to see what part of the sequence does get captured. When you learn what needs to be changed, you can recall the original trigger setup and make changes to it.

See Also

“Branches Taken Stored / Not Stored (State only)” on page 79

“Saving and Recalling Trigger Sequences” on page 67
Incompatible Data Not Loaded

This occurs when loading a configuration file with data that was originally created on a different model of logic analyzer. The configuration files for most logic analyzers can be loaded into different logic analyzer models than they were created on, but the data is not compatible.

Incompatible Timing Data Not Loaded

This occurs when loading a configuration file with data that was originally created on a different model of logic analyzer. Agilent Technologies 16555 and 16556 logic analyzers can load state data from each other, but not timing data.

Incompatible Time Tags Not Loaded

This only occurs when loading a configuration file with data that was originally created on a different model of logic analyzer. Agilent Technologies 16555A and 16556A logic analyzers can load state data from each other except for the time tags. This is also true for the Agilent Technologies 16555D and 16556D. Logic analyzer "A" models and "D" models cannot load each other's data.

Measurement Error: Check Probe Parametrics or Grounding

See “Analyzer Probing Overview” on page 92 or Logic Analysis System and Measurement Modules Installation Guide for details of the logic analyzer connection methods.

Tag Data Has Been Discarded

This message occurs when loading an Agilent Technologies 16555D or 16556D configuration file that contains state data with time tags into an Agilent Technologies 16555A or 16556A. The tags are discarded because there is not enough space in the hardware to store them.

Cannot Read Unrecognized Data

This occurs with Incompatible data not loaded. It means that
the configuration file is corrupted.

**Nothing Happens**

Look for an error message in the *message bar* at the top of the window. Common messages are "slow or missing clock" and "Waiting for trigger".

If the *Run* button briefly grayed-out (and the *Stop* or *Cancel* buttons briefly became active), select the *Window* menu, select the logic analyzer’s slot, then choose the Waveform or Listing display.

**See Also**

- “Slow or Missing Clock” on page 34
- “Waiting for Trigger” on page 37

**Suspicious Data**

**Intermittent Data Errors**

Check for poor connections, incorrect signal levels on the hardware, incorrect logic levels under the logic analyzer’s Config tab, or marginal timing for signals.

**Unwanted Triggers**

If you are using an inverse assembler or a pipeline, triggers can be caused by instructions that were fetched but not executed. To fix, add the prefetch queue or pipeline depth to the trigger address.

The depth of the prefetch queue depends on the processor that you are analyzing, and can be quite deep.

Another solution which is sometimes preferred with very deep prefetch queues is to add writes to dummy variables to your software. Put the instruction just before the area you want to trigger on, then trigger on the actual write to this variable. Although the instruction is prefetched, the analyzer can be set to only trigger when the write is executed.
Testing the Logic Analyzer Hardware

In order to verify that the logic analyzer hardware is operational, run the Self Test utility. The Self Test function of the logic analysis system performs functional tests on both the system and any installed modules.

1. Disconnect all probes of the logic analyzer module.
2. If you have any work in progress, save it to a configuration file. (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)
3. Disconnect all loads, adapters, or preprocessors from the probe cable ends.
4. From the system window, select the System Administration button.
5. Select the Admin tab, then select the Self Test... button. The system closes all windows before starting up Self Test.
6. Select Master Frame. If the module is in an expansion frame, select Expansion Frame.
7. Select the logic analyzer that you want to test.
8. In the Self Test dialog box, select Test All. You can also run individual tests by selecting them. Tests that require you to do something must be run this way.

If any test fails, contact your local Agilent Technologies Sales Office or Service Center for assistance.

See Also

Self Test (see the Agilent Technologies 16700A/B-Series Logic Analysis System help volume)

Agilent Technologies 16557D 140MHz State/500MHz Timing Service Guide
The Sampling Tab

The options under *Sampling* tell the analyzer the overall way in which you want to make a measurement. The options include:

- The acquisition mode.
- The data sample rate.
- How much data before and after the trigger.
- How much data to acquire in all.

**See Also**

“Naming the Analyzer” on page 45
“Turning the Analyzer Off” on page 46
“Setting the Acquisition Mode” on page 42
“Sample Period (Timing Only)” on page 46
“Performing Clock Setup (State only)” on page 42
“Trigger Position Control” on page 47
“Acquisition Depth” on page 41

**Acquisition Depth**

*Acquisition Depth*, located under *Sampling* and also under *Trigger Settings*, sets how much data will actually be acquired. While the Agilent Technologies 16557D logic analyzer has a maximum memory depth of 2M samples in State Mode and 4M in Timing Mode, sometimes you may not want to wait for all that memory to fill up.

The numbers shown in the Acquisition Depth menu are approximations. The combination of *count* tags, pod assignments, and acquisition modes affect what choices are available. Also, the values are memory depth *per channel*. 
Setting the Acquisition Mode

The measurement type affects all other areas of the logic analyzer setup. It is set under the Sampling tab.

If you want the logic analyzer to sample data according to the target system's clock, select State. Each time the clock signal becomes valid, the analyzer will sample data from the system under test.

If you want the logic analyzer to sample the target system independently of its clock, select Timing. Since in timing mode the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. The Agilent Technologies 16557D logic analyzer can be split into two analyzers, but only one of them may be a timing analyzer.

State Mode and Timing Mode offer different options for the acquisition mode field in the top left corner under Controls. The acquisition mode affects the channel width, memory depth, and sample rate.

“State Acquisition Modes” on page 47
“Timing Acquisition Modes” on page 47

Performing Clock Setup (State only)

When you select State Mode, the Clock Setup area appears under the State Mode Controls in Sampling. The Clock Setup contains three controls and a display area. The clocks you specify here control when the analyzer samples your data. Ideally, the logic analyzer’s state clock setup should be identical to the target system’s clock. Differences could result in invalid data.

Mode field

The Mode field lets you select among Master only, Master/slave, and Demultiplex. The default is Master only. When you select the others, another control to set the slave clock appears at the bottom of the
Clock Setup area. It also enables the Pod Clock field under Format.

For more detail on the uses of Master/slave and Demultiplex clocking, see “Clock Modes (State only)” on page 43.

**Advanced Clocking**

Advanced clocking allows you to specify clock qualifiers on individual clock edges instead of the group of clock edges. When you select it, the individual clock channels are replaced by Master Clock... or Slave Clock... Selecting these brings up a dialog that lets you combine edges and qualifiers in more complex Boolean expressions. When you switch from Advanced Clocking to regular clocking, some of the qualifiers are erased.

**Clock Channel Specifiers**

The clock channel specifiers graphically show your clock setup. Edges are ORed ("+") together, and qualifiers are ANDed ("," ) to all edges. To qualify just one of the edges, switch to Advanced Clocking.

All clock channels for the clock setup must be on the pods of the master card of the module, but the pods do not need to be part of the state measurement.

See Also

“Clock Modes (State only)” on page 43

**Clock Modes (State only)**

The Pod Clock field under Format appears when a clock mode other than Master only is selected in Sampling. The Pod Clock field indicates whether a pod’s data lines are to be sampled into memory by the master clock, slave clock, or both (demultiplex).

The Pod Clock field and the clocking arrangement are only available in a state analyzer.

**Master**

Data on all pods assigned to Master Clk is strobed into memory when the status of the clock lines match the clocking arrangement specified for Master in the clock setup.
Slave

Data on a pod designated *Slave Clock* is latched when the status of the slave clock inputs meet the requirements of the slave clocking arrangement. Then, followed by a valid master clock, the slave data is strobed into analyzer memory along with the master data.

If multiple slave clocks occur between master clocks, only the data latched by the last slave clock prior to a valid master clock is strobed into analyzer memory.

Latching Slave Data

Demultiplex

The demultiplex mode is used to store two different sets of data that occur at different times on the same channels. In demultiplex mode, only one pod of the *pod pair* is used, and that pod is selectable (see page 56). Channel assignments are displayed as *Pod* and *Slave Pod*. Assign slave and master data to separate *labels* for easy recognition of the two sets of data.

Both the master and slave clocks are used in the demultiplex mode. When the analyzer sees a match between the slave clock input and the slave clock arrangement, demux slave data is latched. Then, following a valid master clock, the slave data is strobed into analyzer memory along with the master data. If multiple slave clocks occur between master clocks, only the data latched by the last slave clock prior to the master clock is strobed into analyzer memory.
Naming the Analyzer

The Analyzer Name field under Sampling lets you assign a specific name to the analyzer. When you have stored several measurement setups to disk and later reload them, having assigned a specific name to an analyzer can help identify what the setup is for. The analyzer name is also used in the workspace to label the analyzer icons and as part of the title of the analyzer setup window.

There are two analyzers per logic analyzer module. To activate the second one, go to the Workspace window and drag the second analyzer on to the workspace.

The default names for the analyzers are Analyzer<N> and Analyzer<N2>, where N is the slot of the analyzer module.

To Name an Analyzer

1. Select the Analyzer Name field.
2. Enter the new name.

The name now appears below the instrument tool icon in the workspace.
Turning the Analyzer Off

The On and Off checkboxes under the Sampling tab are a shortcut for activating and de-activating the analyzer.

Analyzers come up in the On state. If you select the checkbox, the label changes to Off and the Analyzer Shutdown Options dialog appears.

**Soft**

"Soft" shutdowns have the same effect as though you selected Off in the Type control of the Pod Assignment dialog under Format. The analyzer window remains, but most options are unavailable. Soft shutdowns are easily reversed by selecting the box next to Off.

**Hard**

"Hard" shutdowns have the same effect as deleting the analyzer icon from the workspace. The analyzer window and the windows of its display tools are closed, and the analyzer is removed from the workspace. To turn the analyzer back on, select the analyzer icon in the System window. You will need to restore any complex analysis or display tools.

Sample Period (Timing Only)

Sample Period is used to set the time between data samples. The inverse of sample period is sample rate. Every time a new sample is taken, the analyzer will see updated measurement data. The choices available for sample period depend on the acquisition mode.

If your analyzer is set to timing, the Sample Period control is located under the Sampling tab’s Timing Mode Controls and under the Trigger tab’s Settings sub-tab.

If your analyzer is set to state, the Sample Period control is not available. Its functionality is handled by the Clock Setup.
State Acquisition Modes

135 MHz / 2M State
All pods are available. Memory depth is 2M samples per channel. If time or state count is turned on, memory is halved. To maintain the full 2M samples per channel, leave one pod pair unassigned. State clock speed is up to 135 MHz.

140 MHz / 2M State
All pods are available, but labels may not cross cards. Also, only one of the analyzers available on the module can be used.

Timing Acquisition Modes
In conventional timing acquisition mode the analyzer stores measurement data at each sampling interval.

2M Sample Full Channel 250 MHz
The total memory depth is 2M samples per channel, with data sampled at most every 4 ns.

4M Sample Half Channel 500 MHz
Only one pod of each pod pair is available. The total memory depth is 4M samples, with data sampled at most every 2 ns.

See Also
“Sample Period (Timing Only)” on page 46
“Pod Selection” on page 56

Trigger Position Control
The Trigger Position control, located under Sampling and also Trigger Settings, determines how much data is stored before and after the trigger occurs for all subsequent acquisitions. The trigger point is placed at a specified position relative to the data in memory. The analyzer triggers differently depending on if it is in Timing or State mode.
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The Sampling Tab

Timing Mode

When a Run is started, the analyzer will not look for a trigger until at least the proper percentage of pretrigger data has been stored. After a trigger has been detected, the specified percentage of posttrigger data is stored before the analyzer halts.

State Mode

When the Run is started, the analyzer immediately looks for the trigger condition. The percentage of pretrigger data determines the maximum amount of pretrigger data to save.

The trigger position choices are Start, Center, End, User Defined, or Delay. Delay is only available in timing mode.

- Start
  
The trigger position is set at the starting point of available memory. This process results in maximum posttrigger data and minimum pretrigger data. Note that there will be a small amount of pretrigger data stored.

- Center
  
The trigger position is set at the center point of available memory. This results in half pretrigger data and half posttrigger data.

- End
  
The trigger position is set at the end point of available memory. This results in maximum pretrigger data and minimum posttrigger data. Note that there will be a small amount of posttrigger data stored.

- User Defined
  
When the trigger position is set to User Defined, a trigger position slider appears. Use this slider to set the trigger position any where between 0% and 100%. As the slider is adjusted, the % Post Store indicator shows the amount of data that will be stored after the trigger point.

- Delay
  
This option delays the start of data storage until some time after the trigger. The range of the delay time is affected by the sample period, but it could range between 16 ns to 8 ks.
The Format Tab

Under *Format*, you specify the parts of the target system that you want the logic analyzer to look at. You set up labels to match the buses of the target system, and set the threshold level for the signals. For a *state measurement*, you also adjust the setup and hold time.

For advanced measurements, *Format* is also where you assign pods and specify whether to look at channels on the master, slave, or demultiplexed clock.

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### Common Measurement Controls

- “Labels: Mapping Analyzer Channels to Your Target” on page 55
- “Setting the Pod Threshold” on page 57
- “State Clock Setup/Hold (State only)” on page 58

### Advanced Measurement Controls

- “Assigning Pods to the Analyzers” on page 50
- “Clock Modes (State only)” on page 43
- “Setting Up the Pod Clock” on page 56
- “Pod Selection” on page 56

### See Also

- “Data On Clocks Display” on page 51
- “Activity Indicators” on page 49
- “Assigning Bits to a Label” on page 51
- “Inserting and Deleting Labels” on page 52
- “Turning Labels On and Off” on page 53
- “Reordering the Bits in a Label” on page 54
- “Label Polarity” on page 53

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### Activity Indicators

Activity indicators are the arrows and dashes associated with the pods.
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The Format Tab

They appear in various places, primarily above the column of bit assignment fields in Format and in the Clock Setup area.

When the logic analyzer is properly connected to an active target system, you see arrows in the Activity Indicator displays for each channel. An active channel looks like 

A dash at the top of the activity indicator display indicates that the signal connected to that channel is electrically high (above the threshold voltage). A dash at the bottom indicates that the signal is electrically low. An arrow indicates that the signal is transitioning.

Activity indicators are not affected by label polarity. (see page 53)

You can use these indicators to check whether there is proper probe connection: bits that are stuck high or low may not be properly connected. You can also verify that the signals in your target system are active: bits that are stuck high or low are not crossing the threshold voltage.

Activity indicators are not displayed during an acquisition.

See Also

“Setting the Pod Threshold” on page 57

Logic Analysis System and Measurement Modules Installation Guide for details on probing

Assigning Pods to the Analyzers

The Pod Assignment... button under Format can be used to start the second analyzer on the module and to assign pod pairs.

To Assign Pods to an Analyzer

1. In the Format tab, select the Pod Assignment... button. The Pod Assignment window appears.
2. Drag a pod pair and drop it below the analyzer that you want to assign it to.
3. For pods that you do not want to use, drag and drop them in the Unassigned Pods area. This preserves memory depth when count is turned on.
NOTE:

When both analyzers are turned on, pods 1/2 and 3/4 of the master card cannot be assigned to the same analyzer.

Pods can only be assigned on a per-pair basis to either of the two analyzers. Each pod pair has two clock channels, but only the clock channels of pods on the master card can be used in the analyzer’s clocking setup. These pods do not need to be assigned to that particular analyzer, however.

To turn on an analyzer that is off, select the Off option button and choose State or Timing. (Only one analyzer at a time can be set to Timing.) A second analyzer window appears after a pause for setup.

Data On Clocks Display

The Data On Clocks display column, to the left of the pods’ bit reference line, is a display of all clock inputs available as data channels in the present configuration. This includes those clocks on expander cards, which cannot be used in the clock setup.

To use a clock channel as a data channel, assign the clock bit to a label. Labels containing clock bits cannot be used in range terms where the clock bits span more than one pod pair.

Activity indicators above the clock identifier show signal activity.

See Also

“Assigning Bits to a Label” on page 51

“Activity Indicators” on page 49

Assigning Bits to a Label

The bits in a label correspond to the physical logic analyzer probe channels. When you run the analyzer, data is gathered on all bits (channels) that are assigned to labels. Unassigned bits are inactive.

( * ) (asterisk) indicates an assigned bit.
( . ) (period) indicates an unassigned bit.
( R ) indicates an assigned bit in a reordered label.
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The Format Tab

To Assign Bits

1. Select the bit assignment label to the right of the label name you want to define. Each bit assignment label corresponds to the data pod which is listed above it.
2. Either choose one of the predefined groups, or Individual.
3. In Individual, select the bits to toggle them between an asterisk and a period.

**NOTE:** Labels can have a maximum of 32 channels assigned to them.

Bits assigned to a label are numbered from right to left. The least significant assigned bit on the far right is numbered 0. The next assigned bit to the left is numbered 1, and so on. Labels can contain bits that are not consecutive; however, bits are always numbered consecutively within a label. Above each column of bit assignment fields is a bit reference line that shows you the bit numbers and activity indicators.

**See Also**

“Reordering the Bits in a Label” on page 54
“Activity Indicators” on page 49

Inserting and Deleting Labels

**To Insert Additional Labels**

1. Select the label name button that you want to insert another label next to.
2. Choose Insert before... or Insert after...

**To Delete Labels**

1. Select the button of the label name that you want to delete.
2. Choose Delete.
The bit assignments of deleted labels are not saved. You can make a label inactive but not lose its assignment by turning it off (see page 53) instead.

**Turning Labels On and Off**

You may want to turn off *labels* that you have created so that the label is not displayed. When a label is turned off, its name and bit assignments are preserved.

**To Turn Off a Label**

1. Select the button of the label name that you want to turn off.
2. Choose *Label [ON]* to toggle it off.
   - If the label is the only one, it cannot be turned off or deleted. If there is more than one label but it is the only one on, turning it off turns the first label back on.

**To Turn On a Label**

1. Select the button of the label name that you want to turn on.
2. Choose *Label [OFF]* to toggle it on.

**To Display a Label that was Off**

1. Turn on the label.
2. At the bottom of the window, select the *Apply* button.
   - The label’s data appears in the display windows.

**Label Polarity**

The analyzer uses the label polarity to identify patterns when *triggering* and displaying data.

To change the label polarity, select the polarity field, which toggles between positive (+) and negative (-). Positive polarity means that a high voltage is a logical "1". Negative polarity means that a high voltage is a logical "0".

Changing the label polarity after you have set up other parts of the measurement changes these things:
Chapter 1: Agilent Technologies 16557D 140MHz State/500MHz Timing Logic Analyzer

The Format Tab

- "1" and "0" values flip in trigger terms
- waveforms and bus values (where shown) invert in the Waveform Display tool
- "1" and "0" values flip in the Listing Display tool

Changing the label polarity does not change these things:
- Edge definitions for clock setup and edge terms
- Symbol definitions for the logic analyzer

The default polarity for all labels is positive (+). The various display tools, in particular the Waveform Display tool, all show logical values and are affected by polarity changes.

NOTE: Negative logic is rare in circuits. The main exception at this time is RAMBUS.

Reordering the Bits in a Label

The bit reorder feature allows the channel order, as it appears in the label, to be assigned independently of the physical order. This feature allows the probe tips for each channel to be physically connected where convenient. The Reorder function can then be used to logically rearrange the bits in a label.

NOTE: Reordered labels can not be used as range terms in triggers.

To Reorder the Bits in a Label

1. Select the button of the label name whose bits you want to reorder.
2. Choose Reorder bits.
3. Set the bit order by using one of the following options:
   - To reorder the bits individually, for each channel, enter the number of the bit you want to map the channel to. You can also use the Spin Buttons to scroll through the list of bits.
   - To arrange the bits sequentially, select the option button at the top of the dialog, then choose Default Order.
   - To swap the high and low order bytes or words, select the option
button at the top of the dialog, then choose Big-Endian/Little-Endian.

4. Select the OK button. The label now shows an "R" to indicate bit assignment.

Labels: Mapping Analyzer Channels to Your Target

Labels group and identify related channels, such as buses, in a way that is relevant to your system under test.

A single label can include data and clock channels from more than one pod pair, but these cannot be included in range terms in the trigger specification.

You can define 126 labels per analyzer. Each label can contain up to 32 channels per label.

To Define a Label

1. (Optional) Select the label name button and choose Rename
2. Enter a new name and select the OK button.
3. Assign bits (see page 51) to the label.
4. If necessary, insert more labels (see page 52) in the list.

See Also

“Assigning Bits to a Label” on page 51
“Reordering the Bits in a Label” on page 54
“Inserting and Deleting Labels” on page 52
“Turning Labels On and Off” on page 53
“Label Polarity” on page 53
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The Format Tab

Setting Up the Pod Clock

There is one Pod Clock field for each pod in the machine. It only becomes visible when the Clock Setup under the Sampling tab is set to Master/Slave or Demultiplex. The Pod Clock field is located just below the Pod Threshold in Format.

The Pod Clock field is set to Master Clk by default. Use the Pod Clock field to indicate if the pod's data is to be strobed into memory by the master clock, slave clock, or both, in the demultiplex mode.

When the Pod Clock is set to Demultiplex, only one pod of a pod pair is usable. That pod latches data on both the master and slave clocks, so it appears twice in the label area. To select which pod of a pod pair you want to demultiplex, select the Pod Field.

See Also

“Performing Clock Setup (State only)” on page 42
“Clock Modes (State only)” on page 43 for details on slave and demultiplex clocks
“Pod Selection” on page 56

Pod Selection

The Pod field in Format identifies which pod of a pod pair the settings of the bit assignment field, pod threshold field, and pod clock fields effect. Most of the time it is simply informational. The exceptions are noted below.

Half-Channel Mode

In the half-channel mode, the Pod field becomes a button that you can use to select which pod of a pod pair all pod settings apply to. In the full-channel modes, this field is simply an identifier and is not selectable.
Demultiplex Clock Mode

In the demultiplex clock mode, use the pod field to select which pod of a pod pair is to be used to sample data. In the master or slave clock modes, this field is simply an identifier and is not selectable.

See Also

“Setting the Acquisition Mode” on page 42
“Performing Clock Setup (State only)” on page 42

Setting the Pod Threshold

The pod threshold is a voltage level which the data must cross before the analyzer recognizes it as a change in logic levels. You can specify a threshold level for each pod. The level specified for the master pod that includes the clock is also used for the clock threshold.

To Set the Threshold

1. Under the Format tab, select the threshold field.
   The threshold field is located just below the pod name.
2. In the Pod threshold dialog, choose one of the threshold options described below.
3. If you do not want the change to apply to all pods, select the checked box next to Apply settings to all pods.
4. Select the Close button.

NOTE:
The clock threshold level is the same as the level assigned in the Pod Threshold field.

TTL
The threshold level is +1.5 volts.

ECL
The threshold level is -1.3 volts.
USER
When USER is selected, the threshold level is selectable from -6.0 volts to +6.0 volts.

State Clock Setup/Hold (State only)

Setup/Hold in Format adjusts the relative position of the clock edge with respect to the time period that data is valid. It is only available when the analyzer is set up for a state measurement.

To Change Clock Setup/Hold
1. Select the Setup/Hold button.
2. For each pod pair, choose a Setup/Hold selection from the selection list.
3. Select the OK button.

With a single clock edge assigned, the choices range from 3.5 ns Setup/0.0 ns Hold, to 0.0 ns Setup/3.5 ns Hold. With both edges of a single clock assigned, the choices are from 4.0 ns Setup/0.0 ns Hold, to 0.0 ns Setup/4.0 ns Hold. If multiple clocks are assigned, the choices range from 4.5 ns Setup/0.0 ns Hold, to 0.0 ns Setup/4.5 ns Hold.

The relationship of the clock signal and valid data under the default setup and hold is shown in the figure below for a generic logic analyzer.

![Diagram of clock signal and valid data with default setup and hold](image_url)

Default Setup and Hold
If the relationship of the clock signal and valid data is such that the data is valid for 1 ns before the clock occurs and 3 ns after the clock
occurs, you will want to use the 1.0 setup and 2.5 hold setting.

**Clock Position in Valid Data**
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The Trigger Tab

The Trigger Tab

The Trigger tab is used to set up a sequence that tells the analyzer when to capture data. The key event is the trigger.

The Trigger tab has two main areas:

- On top, tabs of functions and controls to build your trigger
- Beneath the tabs, the current trigger sequence.

Some controls are also located in the logic analyzer window’s menu bar.

- “Understanding Logic Analyzer Triggering” on page 61
- “Setting Up a Trigger” on page 63
- “Inserting and Deleting Sequence Steps” on page 64
- “Editing Sequence Steps” on page 65
- “Setting Up Loops and Jumps in the Trigger Sequence” on page 66
- “Saving and Recalling Trigger Sequences” on page 67
- “Clearing Part or All of the Trigger” on page 68

See Also

- “Overview of the Trigger Sequence” on page 68
- “Trigger Functions” on page 69
- “Working with the User-level Function” on page 76
- “Defining Resource Terms” on page 79
- “Trigger Position Control” on page 47
- “Sample Period (Timing Only)” on page 46
- “Tagging Data with Time or State Tags (State Only)” on page 86
- “Arming Control” on page 86
Understanding Logic Analyzer Triggering

What is a Trigger (see page 61)

What does "Trigger Position" Mean (see page 61)

What can be Used to Specify a Trigger (see page 62)

When to use a Combination, a Branch, or a Level (see page 62)

What is a Trigger

In simplest terms, a trigger is an event that tells the logic analyzer to finish filling its acquisition memory. The memory functions like a conveyor belt: new samples are always coming in, and old samples "falling off" (being overwritten). The logic analyzer has room for 2M samples. When this is full, the only way to fit in new data is to discard the old.

After you specify your trigger sequence and press run, the logic analyzer searches incoming data for events in the trigger sequence. Using the conveyor belt metaphor again, it is like someone tending the conveyor belt who has been told to stop the belt when a certain sample is seen.

The trigger is not like an oscilloscope trigger. Logic analyzers trigger only once per run, even when more than one sample matches the trigger event. Logic analyzer trigger events are like special switches to stop the evaluation process and just fill memory.

What does "Trigger Position" Mean

Because the logic analyzer is continually looking at data from your target system after you select Run, and because the trigger is a single event, you can arrange to collect data relative to it. It is like the person running the conveyor belt is told to stop the belt when the special sample reaches a certain position.

The default trigger position is in the middle. This means there are
approximately as many samples before the trigger as after. You can also arrange for the trigger to be at the beginning of the "conveyor belt" (acquisition memory), the end, or any percentage along it.

**What can be Used to Specify a Trigger**

The trigger sequence can be as simple as one event to look for, or a complicated set of branching levels that loop back and jump around. Both types of triggers use a small set of standard resources.

**Pattern** Pattern terms are things such as $ADDR=0880$ or $R/W=1$. Generally they represent values on buses. You can set patterns to match imprecise events, too. See “Using Bit Pattern Terms” on page 80.

**Range** Range terms match a range of values on a label or bus. For more detail, see “Using Range Terms” on page 81.

**Timer** Timers are started in one sequence level and checked in another. They act like stopwatches. See “Using Timer Terms” on page 83 for more information.

**Edge** Edge terms are similar to edges in oscilloscopes. They are only available for some types of measurements. Edge terms can check for edges on more than one signal at a time, but not all edges have to occur at the same time. To require that, combine edge terms with ANDs.

**Combinations of Terms** To check for more than one type of thing happening in the same sample, combine terms within a sequence level using AND and OR. There are restrictions on exactly which terms can be ANDed and which ORed. The restrictions are covered in “Using Combinations of Terms” on page 84.

**When to use a Combination, a Branch, or a Level**

To check for simultaneous occurrences, use combinations of terms. All the events described by the terms must happen in the same sample.

To take different actions depending on which events happen in a sample, use branches within a sequence level. A branch functions like a set of "if statements" in programming. The sample is checked against
all branches, and the first branch that matches is taken. See “Setting Up Loops and Jumps in the Trigger Sequence” on page 66 for more on branching.

To look for a sequence of events (for example, first look for a memory reference on ADDR, then a certain value on DATA, and when IRQ goes low, trigger) use different sequence levels. When a sample matches the event described in a sequence level, the analyzer goes to the next sequence level and compares the rest of the incoming events. When the logic analyzer reaches the trigger level and finds a sample that matches the trigger event you specify, the logic analyzer triggers.

Setting Up a Trigger

When setting up a trigger sequence, you typically trigger first on a simple pattern or edge. From that point, you execute an iterative process of adding or fine-tuning sequence steps until the analyzer consistently triggers at the desired point.

To Set Up a Trigger

1. Define resource terms. (see page 79)
2. Select the most appropriate trigger function and select the Replace button. (see page 63)
3. Select the sequence level number button and choose Edit. (see page 65)
4. If necessary, insert and edit additional sequence steps. (see page 64)

See Also

“Trigger Functions” on page 69
“Working with the User-level Function” on page 76
“Overview of the Trigger Sequence” on page 68

Selecting a Function to Match Trigger Conditions

Review the list of trigger functions and select the one that matches the event you are looking for. In most cases one of the predefined functions provides a good starting point. If none of the predefined trigger
functions match choose User level at the end of the list.

For a picture corresponding to the trigger function, select the function from the list. The area to the right shows a picture of the function’s effect. The function itself is not inserted into the trigger sequence unless you select the Replace or Insert button.

**See Also**

“Trigger Functions” on page 69

### Inserting and Deleting Sequence Steps

**NOTE:**

For state measurements, the last level of the trigger sequence is always a Store level. It cannot be deleted. For timing measurements, the last level must contain the TRIGGER action.

**To Insert Sequence Steps**

1. Select the sequence level that you want to insert other steps around.
2. Select a trigger function from the list in the Trigger Functions tab.
3. Choose the Insert Before or Insert After button.

**To Delete Sequence Steps**

1. Select the sequence step that you want to delete.
2. Select the Delete button.

**Trigger Sequence Editing Options**

When you select a sequence level, you see a selection menu with choices that allow you to modify the sequence. Choose the option you want from the choices below.

- **Edit**

  Changes the contents of the sequence step. You can change the resource terms or other assignment fields, such as durations and occurrences.

- **Copy**

  Copies the currently selected step. When you copy a level, the new level contains the same function as the original.
The Trigger Tab

- **Replace**
  Replaces the currently selected level with the currently highlighted trigger function.

- **Delete**
  Deletes the level that is currently selected.

- **Insert Before / Insert After**
  Inserts an additional step before or after the selected step.

- **Trigger Level (State only)**
  Makes the current step the trigger level.

- **Default (State only)**
  Only appears in the menu for the last step in a state trigger sequence. The last state always stores to fill memory. Default returns the state to Store anystate.

---

**Editing Sequence Steps**

You can modify the contents of a step in the trigger sequence by editing it.

**To Edit a Sequence Step:**

1. Select the sequence level number button and choose Edit....
2. Select a term name to choose a different term.
   You can also choose negations of terms and combinations of terms.
3. Set the values of the other fields, such as durations and occurrence counts.
4. Select the Close button to close the sequence step editing dialog.

To set the value of a term used in a sequence step, see “Defining Resource Terms” on page 79.

If you are editing a user-level function, refer to:

“Setting Pattern Durations and Occurrence Counts” on page 78 (Timing...
Setting Up Loops and Jumps in the Trigger Sequence

To set up loops and jumps in your trigger sequence, use Branches. Branches are available in most of the Trigger Functions. You may need to break down the functions (see page 75) in order to set up branches.

NOTE:
If either the < or the > durations are selected, only the primary Find or Trigger on selection is available. If the occurs duration is selected, the secondary (Else on) branch becomes available. If the Find field is an edge, only occurs is available.

To Set Up a Branch or Loop

1. Select the Find button and choose the term that you want to branch on. If this term is found in the incoming data, the analyzer will follow this branch and go to the next trigger sequence level.

2. If you want a secondary branch, select the Else on button and choose the term that you want to branch on.

3. Select the goto level option button and select the sequence level that you want to branch to.

If the first branch is taken, the analyzer goes to the next level. If the term in the first branch is not found, the analyzer immediately evaluates the Else on secondary branching term. The analyzer only triggers when the TRIGGER primary branch is taken.

If the Else on term is found, the secondary branch is taken to the designated sequence level, and the occurrence counter is reset even if the branch loops back to the same level. If the Else on term is not
found, the analyzer stays at the same sequence level until one of the two branches is found. If both branches are found true at the same time, the first branch is taken.

See Also

“Breaking Down and Restoring Functions” on page 75
“Branches Taken Stored / Not Stored (State only)” on page 79

Saving and Recalling Trigger Sequences

You can save a trigger sequence independently of configuration files within a session by using Save/Recall. Recalling the stored trigger sequence can change the trigger arming, memory depth, and trigger position as well as the trigger sequence and term definitions. The trigger sequence specification will not change the acquisition mode (full channel vs. half channel).

The Agilent Technologies 16557D logic analyzer can hold up to 10 trigger sequence specifications per mode per machine, for a total of 40 specifications. When you exit your Agilent Technologies 16700A/B session, the trigger sequences are cleared. They can be saved across sessions or be shared across logic analyzers as part of a configuration file, however.

To Save a Trigger Sequence

1. In the Trigger tab, select the Save/Recall subtab.
2. Enter a descriptive name for the trigger sequence in the Title field.
3. Select the Save button.
4. Select a memory location to store the trigger sequence in.

To Recall a Trigger Sequence

1. In the Trigger tab, select the Save/Recall subtab.
2. Select the Recall button.
3. Choose the trigger sequence that you want.
If one of the settings in the recalled trigger sequence conflicts with the acquisition mode, it will be set to the closest setting for that mode.

Clearing Part or All of the Trigger

**To Clear Part or All of the Trigger:**

1. Select the *Trigger* tab.
2. Select *Clear* from the *menu bar*.
3. Choose the option you want from the choices described below:
   - **All**
     
     Clears sequence steps, resource *terms*, resource term names, and trigger position back to their default values. Turns on Count Time.
   - **Sequence Levels**
     
     Resets the *trigger sequence* to the default sequence for the analyzer acquisition mode.
   - **Resource Terms**
     
     Resets all resource term assignment fields, including *labels* and values, back to their default values. The default is usually for all terms to be on the first label, with value *XXXX*.
   - **Resource Term Names**
     
     Resets all the resource term names to their default values, *Pattern1* through *Pattern9* and *Patt10*.
   - **Save/Recall Memories**
     
     Deletes all saved trigger sequence specifications.

Overview of the Trigger Sequence

The *trigger sequence* is a sequence of steps that control the path that the analyzer takes to find the trigger event. The path taken resembles a
flow chart, with each step in the sequence being an opportunity to direct the analyzer’s selection. You can edit the overall trigger sequence by inserting or deleting sequence steps (see page 64).

Each step in the sequence is either a predefined trigger function (see page 69) or a user-level step (see page 76). Both the trigger functions and user-level steps contain variables that you define. The variables, called resource terms (see page 79), represent edges and bit patterns in the data.

When you run the analyzer, it searches for a match between the resource term values and the measurement data. When a match is found, the sequencing continues to the next step, loops back (see page 66) to a previous step, or jumps ahead to another step. Eventually, a path of “true” steps leads to the trigger event.

Each macro uses one or more of the analyzer’s internal sequence levels (see page 76). Each user-level step uses one internal sequence level.

See Also

“Understanding Logic Analyzer Triggering” on page 61 for more detail

“Setting Up a Trigger” on page 63 for actual steps

## Trigger Functions

Trigger functions provide a simple way to set up the analyzer to trigger on common events and conditions. A library of functions is available for both state and timing measurements.

**NOTE:**

Each trigger function requires at least one internal sequence level (see page 76), and in some cases, multiple levels. The number of levels used by each function is described in the references below.

### Timing Trigger Functions

“Basic Timing Trigger Functions” on page 70

“Pattern/Edge Combinations” on page 71

“Time Violations” on page 72

“Timing User Level” on page 70
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The Trigger Tab

**State Trigger Functions**

“Basic State Trigger Functions” on page 73

“Sequence-Dependent Trigger Functions” on page 73

“Time Violations” on page 74

“State User-level” on page 72

**See Also**

“Setting Up a Trigger” on page 63

“Defining Resource Terms” on page 79

“Breaking Down and Restoring Functions” on page 75

**Timing User Level**

The *User level* trigger function allows you to create a custom *trigger sequence* using *terms*, a comparison function, and a secondary branch if the comparison function is *occurs*. This trigger function uses one internal sequence level.

**See Also**

“Working with the User-level Function” on page 76 for more information on the user-defined mode.

**Basic Timing Trigger Functions**

The following basic trigger functions are found in *Trigger Functions* when the analyzer is in *timing* mode. Each function uses one internal sequence level.

- **Find edge.**
  This function becomes true when the edge you have designated is seen. It uses one internal sequence level.

- **Find anystate n times.**
  This function becomes true with the nth state it sees. It uses one internal sequence level. It is equivalent to having the analyzer wait in the sequence level for \((n \times \text{Sample Period})\) seconds.
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The Trigger Tab

- Find nth occurrence of an edge.
  This function becomes true when it finds the designated occurrence of an
  edge you have designated. Note that the 500-MHz trigger sequencer may
  not count edges that occur closer than 2 ns. This function uses one
  internal sequence level.

- Find pattern present/absent for > duration.
  This function becomes true when it finds a pattern you have designated
  that has been present or absent for greater than or equal to the set
duration. It uses one internal sequence level.

- Find pattern present/absent for < duration.
  This function becomes true when it finds a pattern you have designated
  that has been present or absent for less than the set duration. It uses five
  internal sequence levels.

Pattern/Edge Combinations

The following trigger functions are found in Trigger Function when
the analyzer is in timing mode. These predefined functions use a
pattern, edge, or a combination of both as the trigger element. The
functions use either one or two internal sequence levels.

- Find edge AND pattern.
  This function becomes true when a selected edge is seen within the time
  window defined by a pattern you have designated. It uses one internal
  sequence level.

- Find pattern occurring too soon after edge.
  This function becomes true when a pattern you have designated is seen
  occurring within a set duration after a selected edge is seen. It uses two
  internal sequence levels.
The Trigger Tab

- Find pattern occurring too late after edge.
  This function becomes true when one edge you have selected occurs, and
  for a designated period after that first edge is seen, a pattern is not seen. It
  uses two internal sequence levels.

Time Violations

The following trigger functions are found in Trigger Functions when
the analyzer is in timing mode. These trigger functions are specifically
tailored to trigger on events occurring out of a predefined time range.
They use either one or two internal sequence levels.

- Find width violation on a pattern/pulse.
  This function becomes true when the width of a pattern violates minimum
  and maximum width settings you have designated. It uses one internal
  sequence level.

- Find 2 edges too close together.
  This function becomes true when a second selected edge is seen occurring
  within a period you have designated after the occurrence of a first selected
  edge. It uses two internal sequence levels.

- Find 2 edges too far apart.
  This function becomes true when a second selected edge occurs beyond a
  period you have designated after the first selected edge. It uses two
  internal sequence levels.

- Wait t seconds
  This function becomes true after a period you have designated has
  expired. It uses one internal sequence level.

State User-level

The User-level trigger function allows you to create a custom trigger
sequence using terms, a comparison function, and a jump or loop. This
trigger function uses one internal sequence level.

See Also

“Working with the User-level Function” on page 76 for more information on the user-defined mode.

Basic State Trigger Functions

The following basic trigger functions are found in Trigger Functions when the analyzer is in state mode. Each macro uses one internal sequence level.

- Find Pattern n times.
  This function becomes true when it sees a pattern you have designated occurring a designated number of times. The pattern may occur consecutively, but does not have to. It uses one internal sequence level.

- Find anystate n times.
  This function becomes true with the nth state it sees. It uses one internal sequence level. It is equivalent to Wait n external clock states.

- Find pattern2 occurring immediately after pattern1.
  This function becomes true when the first pattern you have designated is seen immediately followed by a second designated pattern. It uses two internal sequence levels.

- Find pattern n consecutive times.
  This function becomes true when it sees a pattern you have designated occurring a designated number of consecutive times. It uses one internal sequence level.

Sequence-Dependent Trigger Functions

The following trigger functions are found in Trigger Functions when the analyzer is in state mode. These functions each trigger on a particular sequence of events.
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The Trigger Tab

- **Find too few states between pattern1 and pattern2.**
  This function becomes true when a designated pattern1 is seen, followed by a designated pattern2, and with fewer than a selected number of states occurring between the two patterns. It uses four internal sequence levels.

- **Find too many states between pattern1 and pattern2.**
  This function becomes true when a designated pattern1 is seen, followed by more than a selected number of states, before a designated pattern2. It uses two internal sequence levels.

- **Find n-bit serial pattern.**
  This function becomes true when a specified serial pattern of n bits is found on the analyzed line. This function uses one internal sequence level for each bit specified in the trigger sequence.

- **Find pattern2 n times after pattern1, before pattern3 occurs.**
  This function becomes true when it first finds a designated pattern1, followed by a selected number of occurrences of a designated pattern2. In addition, if a designated pattern3 is seen anytime while the sequence is not yet true, the sequence starts over. This includes if pattern2’s nth occurrence is at the same time as pattern3, the sequence starts over. It uses two internal sequence levels.

**Time Violations**

The following trigger functions are found in *Trigger Functions* when the analyzer is in *state* mode. These predefined functions are specifically tailored to *trigger* on events occurring out of a predefined time range. These functions use either one or two internal sequence levels.

- **Find pattern2 occurring too soon after pattern1.**
This function becomes true when a designated pattern1 is seen, followed by a designated pattern2, and with less than a selected period occurring between the two patterns. It uses two internal sequence levels.

- Find pattern2 occurring too late after pattern1. This function becomes true when a designated pattern1 is seen, followed by at least a selected period, before a designated pattern2 occurs. It uses two internal sequence levels.

- Wait n external clock states. This function becomes true after a number of user clock states you have designated have occurred. It uses one internal sequence level.

**Breaking Down and Restoring Functions**

When you break down a trigger function, you gain access to all the resource assignment fields and branching options. You can change these fields to change the structure of the trigger sequence. You might need to do this to create a custom trigger sequence or to add jumps.

**To Break Down Trigger Functions**

1. Select *Modify* in the Trigger window menu bar.
2. Choose *Break down functions*. The trigger sequence area changes to show the entire trigger sequence as a series of user-level steps.

The contents of broken down functions are displayed in the long form used in a user-level sequence step. If the function uses two of the analyzer’s internal sequence levels, (see page 76) both levels are separated out and displayed in the trigger sequence area.

**To Restore Functions**

1. Select *Modify* in the Trigger window menu bar.
2. Choose *Restore functions*.

Use *Restore functions* to restore *all* functions to their original
structure. Note that when the functions are restored, all changes are lost and any branching that is part of the original structure is restored.

See Also

“Working with the User-level Function” on page 76 for information on working with functions that are broken down.

How the Internal Sequence Levels Are Used

The analyzer has internal sequence levels that it uses to make up the trigger sequence. There are a total of 16 sequence levels available.

The actual number of levels used in a trigger sequence can vary depending on whether you elect to use predefined trigger functions or use the user-defined steps (see page 76) to construct a more custom trigger sequence.

When you use user-defined steps, all of the internal sequence levels are available. Each user-defined sequence level corresponds to one internal level. The only instance where multiple levels are used is when the < duration is assigned.

When you use predefined trigger functions (see page 69), more than one of the internal sequence levels may be required for a single trigger function. Even though some trigger functions use multiple sequence levels, trigger functions are easier to use, and they are the most efficient way to construct a trigger specification.

Working with the User-level Function

NOTE:

Before you begin to set up user-level sequence steps, note that in most cases one of the predefined trigger functions (see page 69) will work.

You might need to set up a user-level sequence step to accommodate a condition not covered by the functions, or if you need to set up additional loops and jumps in the sequence. Each user-level sequence step has a "fill-in-the-blanks" type statement. You use resource terms to fill in the statement with the appropriate values.
To Set Up a User-Defined Macro

1. In the Trigger Functions tab, select User-level at the end of the list.
2. Select the Replace or Insert button.
3. Select the new sequence level number button; choose Edit.
   A Trigger Sequence Step window appears.
4. For state measurements, select the While storing button; choose the resource term.
   The values represented by this term will be stored in memory while the logic analyzer is evaluating target system data against this step. The default, anystate, stores everything. Nostate stores nothing.
5. Select the Trigger on button or the Find button; choose the resource term.
6. In timing measurements, you have the choice of an occurrence counter or duration. To use the secondary branch, you must set this to occurs.
7. Set the occurrence field or duration.
8. If you want to use a loop or jump:
   a. Select the Else on button; select resource term.
   b. Select the goto level option button; choose a sequence level.
9. If you want to use a timer:
   a. In the appropriate sequence level, start the timer by selecting the Off option button and choosing Start. Timers do not start automatically.
   b. In the Timer tab, assign a time value you want to check against.
   c. To check the value, assign the timer to a resource field either on its own, or as part of a combination.

For more information on the functions available in a user-defined step, refer to:
- “Defining Resource Terms” on page 79
- “Setting Pattern Durations and Occurrence Counts” on page 78 (Timing Only)
- “Using Occurrence Counters” on page 78 (State Only)
• “Setting Up Loops and Jumps in the Trigger Sequence” on page 66
• “Using Timer Terms” on page 83

Setting Pattern Durations and Occurrence Counts

(Timing Only)

When a bit pattern is found during a trigger sequence, you can influence when the term actually becomes “true” by assigning a time duration or an occurrence count.

The (> </occurs) control may not be directly accessible if you are editing a trigger function. To reveal it, break down (see page 75) the function and then follow these instructions.

To Set a Pattern Duration

1. Select the (> </occurs) option button and choose an option.
2. Set the duration or the number of occurrences.

When a greater-than or less-than duration is assigned, the secondary branch (Else on) is not available.

When greater-than (>) is used, the analyzer continues sequence level evaluation only after the resource term has been true for greater than or equal to the amount of duration specified.

When less-than (<) is used, the analyzer continues sequence level evaluation only after the resource term has been true for less than or equal to the amount of duration specified. For each less-than assignment, four internal sequence levels (see page 76) are used.

When occurs is selected, you can set an occurrence count. Use the occurrence counter to delay the trigger sequence evaluation until a resource term has occurred in a designated number of samples. These samples may be interrupted by other values -- they do not need to be consecutive.

Using Occurrence Counters

Use the occurrence counter to delay the trigger sequence evaluation until a resource term has occurred in a designated number of samples.
The samples do not need to be consecutive. Whatever positive number you assign to the counter, the pattern must be seen that number of times before the term becomes true.

If the Else branch becomes true before all specified occurrences of the primary (Trigger on, or Find) branch, the Else branch is taken.

**Branches Taken Stored / Not Stored (State only).** *Branches Taken* sets the analyzer to store, or not to store, the resource terms of the branch that the analyzer followed in the trigger sequence. The Branches Taken control is located in Trigger, under the Settings tab.

Use *Branches Taken* if you want to maximize memory usage but have a complex trigger. With Branches Taken set to stored, you can use store qualifiers to not store the preliminary data ("While storing no state") but still reconstruct the events leading up to your trigger.

When the analyzer is set to *Branches Taken Stored*, all branch events (Find, Else On, or Trigger) are stored when they occur.

When the analyzer is set to *Branches Taken Not Stored*, the branch events will only be stored if the states they represent are included in the *While Storing* qualifier.

The *While storing* field specifies what is being stored in the analyzer's memory before the trigger conditions are met. To set this, select the *While storing* button and choose a pattern or range term for the store qualification.

---

**Defining Resource Terms**

Resource terms are variables that you can use in defining a trigger sequence. The terms available include patterns, edges, ranges, and timers.

When the Agilent Technologies 16557D is configured as a state analyzer, up to fourteen resource terms are available: 10 pattern terms Pattern1 - Pattern9 and Patt10, two range terms, and two timer terms. When configured as a timing analyzer, 16 resource terms are available from the 14 terms already mentioned, plus two
edge terms.

When the module is set up as two analyzers, each resource term can be used by either of the two analyzers, but not both at the same time.

**To Define a Resource Term**

1. In the Trigger tab, select the appropriate subtab to bring the group of terms forward.

2. Optional - Highlight the term name and enter a new name.
   For Timer terms, set the time value and skip the remaining steps.

3. Optional - Select the label button to the right of the term name and choose Replace.

4. Select the label that you want to use.

5. Optional - add more labels (see page 85) to the term.

6. Optional - Set the numeric base.

7. Select the term value field, to the right of the label name.

8. For pattern and range terms, enter the term value. For edge terms, assign edges or glitches to appropriate bits.

**See Also**

“Using Bit Pattern Terms” on page 80
“Using Edge Terms” on page 82
“Using Range Terms” on page 81
“Using Combinations of Terms” on page 84
“Using Timer Terms” on page 83
“Adding and Deleting Labels for Terms” on page 85
“Numeric Base” on page 85

**Using Bit Pattern Terms**

Bit pattern resource terms can be set to match a numeric value or bit pattern on a group of data channels such as a bus. In order for a pattern to be found by the analyzer, the input data must match all bits of the pattern that are not defined as Don’t Cares (X). Patterns can also be
used in a negated form.

To Define a Pattern Term

1. Select the label name button to the right of the term name and choose the label that you want to use.
2. If necessary, add more labels (see page 85) to the term.
3. Select the term value field, to the right of the label name.
4. Enter the pattern for each label.
   Depending on the base setting, such as hex or octal, some characters will not be accepted. Don’t cares are indicated by an X.

Tip

Right-click on any of the bit pattern value fields to quickly assign the pattern term to a preset value. Clear (=X) sets the value to all X (don’t cares). Set (=1) sets the value to all 1s. Reset (=0) sets the value to all 0s.

Using Range Terms

Range terms bracket groups of data values between upper and lower boundaries that you assign. The range term becomes true when the data is numerically between or on the two specified boundaries.

The labels used by a range must be contained in a single pod pair, with no clock channels or re-ordered bits allowed.

To Define a Range Term

1. Select the label name button to the right of the term name and choose the label that you want to use.
   Only one label can be used at a time for range terms.
2. Select the lower value field, to the right of the label name.
3. Enter the pattern for the low value of the range.
4. Select the upper value field, to the right of the label name.
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The Trigger Tab

5. Enter the pattern for the upper value of the range. Depending on the base setting, such as Hex or Octal, some characters will not be accepted.

![Pattern and Range Table]

Tip

Right-click on either of the value fields to quickly assign the value to a preset value. Set (=1) sets the value to all 1s. Reset (=0) sets the value to all 0s.

Using Edge Terms

Edge terms are only available in timing mode. You can set an edge term to match transitions or glitches on one or more channels. When you specify an edge or glitch on more than one channel, the analyzer logically ORs the edges together. When the analyzer sees a transition that matches any of the ones specified in the edge term, the term becomes true. If you must have both edges occur in the same sample, assign the edges to different terms and combine them (see page 84) with an AND.

The following edge choices are available for each bit:

- Rising edge (*)
- Falling edge (*)
- Either rising or falling
- Glitch (*)

To Define an Edge Term

1. Select the label name button and choose the label that you want to use.
2. Select the edge value button, to the right of the label name.
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The Trigger Tab

3. Set the edge or glitch for each channel. Don’t cares are indicated by a (\).

NOTE: After you close the edge term assignment dialog, you may see $ indicators in the term value field. This symbol indicates that the value can’t be displayed in the selected base. Choose Binary base to see the actual assignments.

Using Timer Terms

Timers are like other resource terms in that they are either true or false. They are unlike other terms, however, in that they are controlled within the trigger sequence and act like a stopwatch. When a timer reaches its assigned count (expires), it becomes true. When a timer expires or stops, its count resets to zero.

Timers can be set to Start, Stop, Pause, or Continue as the analyzer enters a trigger sequence level. The two timers are global, so each sequence level except the first has the ability to control the same timer. As more sequence levels are added, the timer status in the new levels defaults to Off. If a timer is paused in one level, it must be continued in another level before it will be restarted. If the trigger sequence returns to the same sequence level again, the timer will be restarted.

Each Timer term can be used by either of the two analyzers, but not both.

To Assign a Time Value to the Timer Terms

1. Select the Timer subtab in the Trigger tab.
2. Select the timer value field, next to the timer name.
3. Enter a timer value.
4. Use the up/down arrow buttons to scroll through timer values.

The minimum value a timer can have is 400 ns, which is also the default value.

To Include a Timer in a Trigger Sequence

1. Assign a time value to the timer you want to use.
2. Select the sequence level you want to use it in, and choose Edit....
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The Trigger Tab

Timer control is not available in the first sequence level.

3. Select the Off option button at the bottom of the edit dialog box and choose Start.
   If the other analyzer is already using a timer, it won’t appear in this analyzer’s edit dialog.

4. Select the event field where you want to use the timer.

5. Choose either Timer or Combo…
   Use Combo for cases such as an edge occurring after so many nanoseconds.

6. In the other trigger levels, you can Start, Pause, and Continue the timer.
   When a timer reaches its assigned value, it automatically stops.

See Also

“Using Combinations of Terms” on page 84

Using Combinations of Terms

Resource terms can be used in combinations. Combinations use the logical AND, NAND, OR, NOR, and XOR functions to combine predefined resource terms.

A combined term is evaluated as a single events. Components that are ANDed together must all occur in the same sample. Ones that are ORed together only require one of the components to happen.

If you intend for the logic analyzer to decide between two actions, use branches instead of combined terms. If you want the logic analyzer to find the terms in sequence, use different levels or a trigger function in the trigger sequence.

To Set Up a Combination

1. Edit the sequence step (see page 65) that you want a combination term to appear in.

2. Select the resource term assignment field that you want to make into a combination.

3. Choose Combo… from the menu of resource terms.

4. In the Combination dialog, select the On/Off/Not option button for each term that you want to use and select On or Not.
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The Trigger Tab

Not selects the logical negation of the term.

5. Select the logical operator buttons and choose a logic operation. Not all operations are available at all levels of the combination tree.

NOTE:
The combination of terms is now inserted into the term assignment field. If the term is too long to fit, the display is truncated.

Adding and Deleting Labels for Terms

Labels are defined in Format, after which they are available throughout the other analyzer areas and attached display tools.

When you use more than one label to define a trigger term, the term conditions must be true on both labels for the term to be true.

To Add a Label to a Resource Term

1. Select the label name button.
2. Choose Insert.
3. Select the label that you want to add to the resource term.

To Delete a Label from a Resource Term

1. Select the label name button.
2. Choose Delete.

Numeric Base

All labels have a numeric base field next to them. The base choices are Binary, Octal, Decimal, Hex, ASCII, Symbol and Twos Complement.

To Change the Numeric Base

1. Select the base option button.
2. Choose the base that you want.

NOTE:
If the numeric base is changed in one window, the base in other windows may not change accordingly. For example, the base assigned to symbols is unique, as is the base assigned in the Listing window.
Tagging Data with Time or State Tags (State Only)

The Count field under Settings in Trigger accesses a selection menu which is used to stamp the data at each memory location with either a Time tag or a State Count tag. The tags reduce the memory depth by half. To retain the full memory depth when using time or state tags leave one pod pair unassigned.

**State Count**

When the State Count option is selected, numbered tags are placed on all selected data. Pre-trigger data has negative numbers and post-trigger data has positive numbers. You select the data to be tagged when you turn on State Count. A field appears to the right of States that lets you define patterns.

State tag numbering can be set either relative to the previous tagged sample or absolute from the trigger point. Selecting Absolute or Relative is done by toggling the Absolute/Relative field in the Listing Display window.

**Time Count**

Time Count places time tags on all data. Pre-trigger data has negative time numbers and post-trigger data has positive time numbers. Time tag numbering is set to be either relative to the previous memory location or absolute from the trigger point. The time tag resolution is 4 ns.

**Arming Control**

An instrument must be armed before it can look for its trigger. When you Run an instrument, it is armed immediately. When using logic analyzer modules that provide two separate analyzers, you can set one analyzer to arm the other within the same module by selecting Arming Control... under Settings in Trigger.
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The Trigger Tab

Selecting the *Arming Control...* button brings up the *Machine Arming Tree* dialog. In this dialog you can set what starts each analyzer, and which one sends a signal to *Arm Out*. *Arm Out* is used to send signals to other instruments in the frame, or sent to *Port Out*. *Port Out* can be used to control additional instruments external to the logic analysis system.

To change the source of *Arm In* or the destination of *Port Out*, use the Intermodule dialog (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume).

### Setting One Analyzer to Arm the Other

This procedure assumes you have both analyzers turned on. The second analyzer can be turned on by dragging it onto the workspace in the Workspace window.

1. Under the Trigger tab, select the *Settings* subtab.
2. Select the *Arming Control...* button.
3. Select the box of the machine that you want to have wait for its arm signal.
4. In the *armed by* menu, select the other machine. The arming signal path forms a tree in the Machine Arming Tree dialog.
5. Set the sequence level number to the trigger sequence level that will wait for the arm signal. It does not have to be the same as the trigger level.
6. Select the *Close* button.

**NOTE:**
If the trigger sequence does not pass through the level containing the *wait for arm* term, the trigger will not wait for the arming signal.

### See Also

- Overview - Multiple Instrument Configuration (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)
- Overview - Multiple Machine Configuration (see the *Agilent Technologies 16700A/B-Series Logic Analysis System* help volume)
Specifications and Characteristics

NOTE:

Definition of Terms

To understand the difference between specifications (see page 88) and characteristics (see page 88), and what gets a calibration procedure (see page 89) and what gets a function test (see page 89), refer to appropriate links within this note.

“Agilent Technologies 16557D Logic Analyzer Specifications” on page 89
“Agilent Technologies 16557D Logic Analyzer Characteristics” on page 90

What is a Specification

A Specification is a numeric value, or range of values, that bounds the performance of a product parameter. The product warranty covers the performance of parameters described by specifications. Products shipped from the factory meet all specifications. Additionally, the products sent to Agilent Technologies Customer Service Centers for calibration and returned to the customer meet all specifications.

Specifications are verified by Calibration Procedures.

What is a Characteristic

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics describe performance that is typical of the majority of a given product, but not subject to the same rigor associated with specifications.

Characteristics are verified by Function Tests.
What is a Calibration Procedure

Calibration procedures verify that products or systems operate within the specifications. Parameters covered by specifications have a corresponding calibration procedure. Calibration procedures include both performance tests and system verification procedure. Calibration procedures are traceable and must specify adequate calibration standards.

Calibration procedures verify products meet the specifications by comparing measured parameters against a pass-fail limit. The pass-fail limit is the specification less any required guardband.

The term "calibration" refers to the process of measuring parameters and referencing the measurement to a calibration standard rather than the process of adjusting products for optimal performance, which is referred to as an "operational accuracy calibration".

What is a Function Test

Function tests are quick tests designed to verify basic operation of a product. Function tests include operator’s checks and operation verification procedures. An operator’s check is normally a fast test used to verify basic operation of a product. An operation verification procedure verifies some, but not all, specifications, and often at a lower confidence level than a calibration procedure.

Agilent Technologies 16557D Logic Analyzer Specifications

The specifications are the performance standards against which the product is tested. These specifications apply only to the Agilent Technologies 16557D 140MHz State/500MHz Timing logic analyzer:

- Threshold Accuracy: +/- (100mV + 3% of threshold setting)
- Setup/Hold Time for 1- through 4-card modules:
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Specifications and Characteristics

*Single Clock, Single Edge: 3.0/0.0 ns through -0.5/3.5 ns, adjustable in 500-ps increments
Minimum Master-to-Master Clock Time: 7.142 ns

*Single Clock, Multiple Edge: 3.5/0.0 ns through -0.5/4.0 ns, adjustable in 500-ps increments
Minimum Master-to-Master Clock Time: 7.142 ns

*Multiple Clock, Multiple Edge: 4.0/0.0 ns through -0.5/4.5 ns, adjustable in 500-ps increments
Minimum Master-to-Master Clock Time: 7.142 ns

5-card modules have the same setup/hold time, but 10.0 ns minimum master-to-master clock time.

* Specified for an input signal VH=-0.9 V, VL=-1.7 V, threshold=-1.3 V, slew rate=1 V/ns

Agilent Technologies 16557D Logic Analyzer Characteristics

The characteristics are not specifications, but are included as additional information.

General information
- Channel Counts:
  1-card module 64 data, 4 clock
  2-card module 132 data, 4 clock
  3-card module 200 data, 4 clock
  4-card module 268 data, 4 clock
  5-card module 336 data, 4 clock

- Memory Depth:
  Half Channel 4 M samples per channel
  Full Channel 2 M samples per channel

Half Channel mode is only available for timing analysis.

Probes (at end of flying lead set)
- Input Resistance: 100 Kohm, +/- 2%
- Input Capacitance: ~8 pF
- Minimum Voltage Swing: 500 mV peak-to-peak
- Maximum Voltage: +/- 40 V peak, CAT I
- Threshold Range: +/- 6.0 V, adjustable in 50-mV increments
- Power through pod cables: 1/3 amp to a maximum of 5 V per pod

State Analysis
- Maximum State Clock Speed: 1-4 cards: 140 MHz
  5 cards: 100 MHz
- *Minimum Setup/Hold Time: 3.0/0.0 ns through -0.5/3.5 ns, adjustable in 500-ps increments
- Minimum State Clock Width: 3.5 ns
- State Clocks: 4
- State Clock Qualifiers: 4
- **Time Tag Resolution: 8 ns
- Maximum Time Count Between States: 34 seconds
- **Maximum State Tag Count: 4.29e9

* Specified for single-edge, single-clock acquisition. Single-clock, multi-edge setup/hold window is 3.5 ns. Multi-clock, multi-edge setup/hold window is 4.0 ns.
** When all pods are being used, time or state tags halve the memory

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Specifications and Characteristics

Timing Analysis
- Maximum Conventional Timing Rate:
  - Half Channel: 500 MHz
  - Full Channel: 250 MHz
- Sample Period Accuracy: 0.01% of sample period
- Channel-to-Channel Skew: 2 ns, typical
- Time Interval Accuracy: \( \pm (\text{sample period} + \text{channel-to-channel skew} + 0.01\% \text{ of time interval reading}) \)

Triggering
- State Sequence Levels: 12
- Timing Sequence Levels: 10
- Maximum Occurrence Count Value: 1,048,575
- Pattern Recognizers: 10
- Range Recognizers: 2
- Range Width: 32 bits each
- Timers: 2
- Timer Value Range: 400 ns to 500 seconds
- Glitch/Edge Recognizers: 2 (timing only)
- Minimum Detectable Glitch: 3.5 ns

Power Requirements
All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Operating Environment Characteristics
- Indoor use only.
- Temperature
  - Instrument: 0 to 40 degrees C (+32 to 122 degrees F)
  - Probe lead sets and cables: 0 to 65 degrees C (+32 to 149 degrees F)
- Humidity
  - Instrument, probe lead sets, and cables: up to 95% relative humidity at 40 degrees C (+122 degrees F)
  - Altitude: To 4600 m (15,000 ft)
- Vibration
  - Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.3 g (rms)
  - Nonoperating: Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5-minute resonant dwell at 4 resonances per axis.

Reliability is enhanced when operating within the following ranges:
- Temperature: +20 to 35 degrees C (+68 to 95 degrees F)
- Humidity: 20% to 80% non-condensing

Storage
Store or ship the logic analyzer in environments with the following limits:
- Temperature: -40 to +75 degrees C
- Humidity: up to 90% at 65 degrees C
- Altitude: up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.
Analyzer Probing Overview

The figures below show a variety of simple probing connections. The specific probe type, number of probes, and location on the target circuit depends on your particular measurement.

For equivalent circuit diagrams and pinouts, see the description of the probe type in the Logic Analysis System and Measurement Modules Installation Guide. If you have misplaced the Logic Analysis System and Measurement Modules Installation Guide, you can download the latest version from the Web at <URL: http://www.agilent.com/find/LogicAnalyzer-Manuals/>.

**Probe Lead-to-Board Connection**

The standard lead set plugs directly into any .1-inch grid with 0.026 to 0.033-inch diameter round pins or 0.025-inch square pins. All probe tips work with the Agilent Technologies 5059-4356 surface mount grabbers and the Agilent Technologies 5959-0288 through-hole grabbers.
Both the 01650-63203 and the E5346A adapters include termination for the logic analyzer. The 01650-63203 termination adapter plugs into a 2 x 10 pin header with 0.1 inch spacing. The E5346A high-density adapter connects to an AMP "Mictor 38" connector. If possible, use support shrouds around the Mictor connector to relieve strain and improve connections.

**Direct Pod-to-Board Connection**

If you provide proper termination as part of the target board, you can plug the pod directly into the ©3M 2520-series, or similar alternative connector. Suggested termination is shown in the *Logic Analysis System and Measurement Modules Installation Guide*.

Also use this termination with the Agilent Technologies E5351A high-density, non-terminated adapter.

**Pod-to-Analysis Probe Connection**

Analysis probes (formerly called preprocessors) are microprocessor-specific interfaces that make it easier to probe buses. Generally,
analysis probes consist of a circuit board that attaches to the microprocessor (possibly through an adapter) and a configuration file. The configuration file sets up the logic analyzer’s clocks and labels correctly, and may include an inverse assembler. The circuit board provides access to logical groups of pins through headers designed to connect directly to the logic analyzer.

The easiest way to set up a measurement with an analysis probe is the Setup Assistant. (see the Setup Assistant help volume) The Setup Assistant asks you questions about your measurement and then shows you just the information you need to set up the probe correctly. It also loads the proper configuration files.
The Symbols Tab

The Symbols tab offers control of the symbols capabilities. Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:

- Object File Symbols. These are symbols from your source code and symbols generated by your compiler.
- User-Defined Symbols. These are symbols you create.

To load symbols, see:
- “To Load Object File Symbols” on page 97
- “To Load User-Defined Symbols” on page 110

Symbols are available for all state and timing analyzers. Each label listed in the Format menu can have its own group of symbols associated with it.

- “User-Defined Symbols” on page 109
- “Setting Up Object File Symbols” on page 97
- “Using Symbols In The Logic Analyzer” on page 111
- “Displaying Data in Symbolic Form” on page 96
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Displaying Data in Symbolic Form

You can display data in symbolic form in some of the display tools, such as the Listing display and the Waveform display.

**To View Symbolic Values in a Waveform Display**

1. Select the label name where you want to display symbolic values.
2. Choose *Properties*….
3. In the Properties dialog:
   - Set ShowValue to *On*.
   - Set Base to *Symbols* or *Line #s*.
   - Select the OK button.

   The symbolic names for the values now appear in the overlayed bus waveform.

**To View Symbolic Values in a Listing Display**

1. Select the numeric base of the label where you want to display symbolic values.
2. Set the numeric base to *Symbols* or *Line #s*.
   - The symbolic names for the values now appear instead of numeric data.
Setting Up Object File Symbols

Object file symbols can include variable names, procedure or function names, and source file names with line numbers. The linkage between symbol names and address or data values comes from one of two sources:

- Object files that are created by your compiler/linker.
- ASCII symbol files you create with a text editor.

**To use object file symbols**

1. Generate an object file with symbolic information using your software development tools.
2. If your language tools cannot generate object file formats that are supported by the logic analyzer, create an ASCII symbol file (see page 101).
3. Load the object file (see page 97) or ASCII symbol file into the logic analyzer.
4. If necessary, relocate sections of your code (see page 99).

**See Also**

- “Using Symbols In The Logic Analyzer” on page 111
- “Symbol File Formats” on page 100

To Load Object File Symbols

1. Select the *Symbol* tab and then the *Object File* tab.
2. Select the label name you want to load object file symbols for. In most cases you will select the label representing the address bus of the processor you are analyzing.
3. Specify the directory to contain the symbol database file (.ns) in the field under, *Create Symbol File (.ns) in This Directory*. Select the *Browse*... button if you wish to find an existing directory name.
4. In the **Load This Object/Symbol File For Label** field, enter the object file name containing the symbols. Select the **Browse...** button to find the object file and select the **Load** button in the Browser dialog. If your logic analyzer is NFS mounted to a network, you can select object files from other servers.

**To reload object file symbols**

1. Select the object file/symbol file to reload from the **Object Files with Symbols Loaded For Label** field.

2. Select the **Reload** button.

**Value update**

The values of the object file symbols being used as terms or as SPA state-interval ranges will be updated automatically each time the object file symbols are reloaded.

**Configuration file save**

The name of the current object file is saved when a configuration file is saved. The object file will be reloaded when the configuration is loaded.

**Multiple files**

You can load the same symbol file into several different analyzers, and you can load multiple symbol files into one analyzer. Symbols from all the files you load will appear together in the object file symbol selector that you use to set up resource terms.

**Object file versions**

During the load process, a symbol database file with a `.ns` extension will be created by the system. One `.ns` database file will be created for each symbol file you load. Once the `.ns` file is created, the Symbol Utility will use this file as its working symbol database. The next time you need to load symbols into the system, you can load the `.ns` file explicitly, by placing the `.ns` file name in the **Load This Object/Symbol File For Label** field.

If you load an object file that has been loaded previously, the system will compare the time stamps on the `.ns` file and the object file. If the
Setting Up Object File Symbols

object file is newer, the .ns file will be created. If the object file has not been updated since it was last loaded, the existing .ns file will be used.

See Also

“Using Symbols In The Logic Analyzer” on page 111
“Symbol File Formats” on page 100

Relocating Sections of Code

Use this option to add offset values to the symbols in an object file. You will need this if some of the sections or segments of your code are relocated in memory at run-time. This can occur if your system dynamically loads parts of your code so that the memory addresses that the code is loaded into are not fixed.

To Relocate a Single Section of Code

1. Select the Symbol tab and then the Object File subtab.
2. Select the Relocate Sections... button.
3. In the Address column, select the address you wish to relocate.
4. In the Edit selected section field, enter the new address.
5. Select Apply Edit.
6. Repeat steps 3 through 5 above for any other sections to be relocated.
7. Select the Close button.

To Relocate All Sections of Code

1. Select the Symbol tab and then the Object File subtab.
2. Select the Relocate Sections... button.
3. Enter the value you wish to use in the Offset all selections by field.
4. Select the Apply Offset button.
5. Select the Close button.
To Delete Object File Symbol Files

1. Select the *Symbol* tab, and then the *Object File* subtab.

2. Select the file name you want to delete in the text box labeled, *Object Files with Symbols Loaded For Label*.

3. Select the *Unload* button.

Symbol File Formats

The logic analysis system can read symbol files in the following formats:

- OMF96
- OMFx86
- IEEE-695
- ELF/DWARF
- ELF/stabs
- TI COFF

For ELF/DWARF1, ELF/stabs, and ELF/stabs/Mdebug files, C++ symbols are demangled so that they can be displayed in the original C++ notation. To improve performance for these ELF symbol files, type information is not associated with variables. Hence, some variables (typically a few local static variables) may not have the proper size associated with them. They may show a size of 1 byte and not the correct size of 4 bytes or even more. All other information function ranges, line numbers, global variables and filenames will be accurate. These behaviors may be changed by creating a readers.ini (see page 106) file.

See Also

“Creating ASCII Symbol Files” on page 101

“Creating a readers.ini File” on page 106
Creating ASCII Symbol Files

If your language tool chain does not produce object files in a supported format, you can create an ASCII symbol file to define symbols. You can also use an ASCII symbol file to define symbols that are not included in your object file.

You can create an ASCII symbol file using any text editor that supports ASCII format text. Each entry in the file you create must be a string of ASCII characters consisting of a symbol name followed by an address or address range. The address or address range must be a hexadecimal number. It must appear on the same line of the text file as the symbol name and it must be separated from the symbol name by one or more blank spaces or tabs. Address ranges must be in the following format:

```
beginning address..ending address
```

Two formats are available for creating ASCII symbol files:

```
“Simple Format” on page 101
```

```
“Record Header Format” on page 101
```

**NOTE:**

It is possible to generate ASCII symbol files from the symbol or load map output of most language tools.

**Simple Format**

An ASCII symbol file can be a simple list of name/address pairs.

**Example**

```
main     00001000..00001009
test     00001010..0000101F
var1     00001E22     #this is a variable
```

This example defines two symbols that correspond to address ranges and one point symbol that corresponds to a single address.

**Record Header Format**

An ASCII symbol file can be divided into records using key words,
called *record headers*. The different records allow you to specify different kinds of symbols, with differing characteristics. An ASCII symbol file can contain any of the following kinds of records:

- “Start Address” on page 103
- “Sections” on page 103
- “Functions” on page 103
- “Variables” on page 105
- “Source Line Numbers” on page 104
- “Comments” on page 105

The record headers must be enclosed in square brackets, like this: [HEADER]. If no record header is specified, the lines following are assumed to be symbol definitions in one of the VARIABLES formats:

```
variable   address
variable   start..end
variable   start address   size
```

**Example**

Here is an ASCII symbol file that contains several different kinds of records.

```
[SECTIONS]
prog      00001000..0000101F
data      40002000..40009FFF
common    FFFF0000..FFFF1000

[FUNCTIONS]
main      00001000..00001009
test      00001010..0000101F

[VARIABLES]
total     40002000  4
value     40008000  4

[SOURCE LINES]
File: main.c
10       00001000
11       00001002
14       0000100A
22       0000101E
```
Start Address. Format

[START ADDRESS]
address

address - The address of the program entry point, in hexadecimal.

Example

[START ADDRESS]
00001000

Functions. Use FUNCTIONS to define symbols for program functions, procedures or subroutines.

Format

[FUNCTIONS]
func_name start..end

func_name - A symbol representing the function name.

start - The first address of the function, in hexadecimal.

end - The last address of the function, in hexadecimal.

Example

[FUNCTIONS]
main 00001000..00001009
test 00001010..0000101F

Sections. Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

Format

[SECTIONS]
section_name start..end attribute

section_name - A symbol representing the name of the section.
Setting Up Object File Symbols

start - The first address of the section, in hexadecimal.

dend - The last address of the section, in hexadecimal.

attribute - (optional) Attribute may be one of the following:

NORMAL (default) - The section is a normal, relocatable section, such as code or data.

NONRELOC - The section contains variables or code that cannot be relocated. In other words, this is an absolute segment.

Example

[SECTIONS]
prog           00001000..00001FFF
data           00002000..00003FFF
display_io     00008000..0000801F  NONRELOC

NOTE:
If Section definitions are used in an ASCII symbol file, any subsequent Function or Variable definitions must fall within the address ranges of one of the defined Sections. Those Functions and Variables that do not will be ignored by the Symbol Utility.

Source Line Numbers . Use SOURCE LINES to associate addresses with lines in your source files.

Format

[SOURCE LINES]
File: file_name
line#  address

file_name - The name of a file.

line# - The number of a line in the file, in decimal.

address - The address of the source line, in hexadecimal.

Example

[SOURCE LINES]
File: main.c
10       00001000
11       00001002
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Setting Up Object File Symbols

See Also

Using the Source Viewer (see the Listing Display Tool help volume)

Variables. You can specify symbols for variables using:

- The address of the variable.
- The address and the size of the variable.
- The range of addresses occupied by the variable.

If you give only the address of a variable, the size is assumed to be 1 byte.

Format

\[[VARIABLES]\]

\[var\_name \quad start \ [size]\]

\[var\_name \quad start..end\]

\[var\_name\] - A symbol representing the variable name.

\[start\] - The first address of the variable, in hexadecimal.

\[end\] - The last address of the variable, in hexadecimal.

\[size\] - (optional) The size of the variable, in bytes, in decimal.

Example

\[[VARIABLES]\]

subtotal \quad 40002000 \quad 4

total \quad 40002004 \quad 4

data\_array \quad 40003000..4000302F

status\_char \quad 40002345

Comments. Any text following a \# character is ignored by the Symbol Utility. The \# can be used to comment a file. Comments can appear on a line by themselves, or on the same line, following a symbol entry.

Format

\[#comment\ text\]
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Setting Up Object File Symbols

Example

#This is a comment

Creating a readers.ini File

You can change how an ELF/Dwarf, ELF/Stabs, Ticoff or Coff/Stabs symbol file is processed by creating a reader.ini file.

1. Create the reader.ini file on your workstation or PC.
2. Copy the file to /logic/symbols/readers.ini on the logic analysis system.

Reader options

<table>
<thead>
<tr>
<th>C++Demangle</th>
</tr>
</thead>
<tbody>
<tr>
<td>1= Turn on C++ Demangling (Default)</td>
</tr>
<tr>
<td>0= Turn off C++ Demangling</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C++DemOptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>803= Standard Demangling (Default Elf/Dwarf)</td>
</tr>
<tr>
<td>203= GNU Demangling          (Default Elf/Stabs)</td>
</tr>
<tr>
<td>403= Lucid Demangling</td>
</tr>
<tr>
<td>800= Standard Demangling without function parameters</td>
</tr>
<tr>
<td>200= GNU Demangling without function parameters</td>
</tr>
<tr>
<td>400= Lucid Demangling without function parameters</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MaxSymbolWidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>80= Column width max of a function or variable symbol</td>
</tr>
<tr>
<td>Wider symbols names will be truncated. (Default 80 columns)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ReadElfSection</th>
</tr>
</thead>
<tbody>
<tr>
<td>2= Process all globals from ELF section (Default)</td>
</tr>
<tr>
<td>1= Get size information of global and local variables Symbols for functions will not be read, and only supplemental information for those symbols in the Dwarf or Stabs section will be read.</td>
</tr>
<tr>
<td>0= Do not read the Elf Section</td>
</tr>
</tbody>
</table>

If a file only has an ELF section this will have no effect and the ELF section will be read completely. This can occur if the file was created without a "generate debugger information" flag (usually -g). Using the -g will create a Dwarf or Stabs debug section in addition to the ELF section.
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Setting Up Object File Symbols

Dwarf1NoType

1= Use the new fast symbol reader for Dwarf1 (Default)
0= Use the previous version of the symbol reader

This symbol reader will be slow and may not be able to process all files. In addition the older symbol reader does not do C++ demangling. This symbol reader does process type information, so the sizes of local static and global variables will be processed.

Do not use this option unless you are having trouble reading the symbol file. This option will most likely be deleted in the future.

StabsType

StabsType=0 Reader will determine stabs type (Default)
StabsType=1 Older style stabs
(Older style stabs have individual symbol tables for each file that was linked into the target executable, the indexes of each symbol table restart at 0 for each file.)
StabsType=2 Newer style stabs
(New style stabs have a single symbol table where all symbols are merged into a large symbol array).

ReadOnlyTicoffPage

ReadOnlyTicoffPage tells the ticoff reader to read only the symbols associated with the specified page (as an example ‘ReadOnlyTicoffPage=0’ reads only page 0 symbols). A value of -1 tells the ticoff readers to read symbols associated with all pages.

ReadOnlyTicoffPage=-1 Read all symbols associated with all ticoff pages (Default)
ReadOnlyTicoffPage=p Read only symbols associated with page ‘p’ (where p is any integer between 0 and n the last page of the object file).

AppendTicoffPage

AppendTicoffPage tells the ticoff reader to append the page number to the symbol value. This assumes that the symbol value is 16-bits wide and that that page number is a low positive number which can be ORed into the upper 16 bits of an address to create a new 32-bit symbol address. For example, if the page is 10 decimal and the symbol address is 0xF100 then the new symbol address will be 0xAF100.

AppendTicoffPage=1 Append the ticoff page to the symbol address
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Setting Up Object File Symbols

AppendTicoffPage=0  Do not append the ticoff page to the symbol address (Default)

Examples

Example for Elf/Dwarf

[ReadersElf]
C
C
MaxSymbolWidth=60
ReadElfSection=1
Dwarf1NoType=1

Example for Elf/Stabs

[ReadersElf]
C
C
MaxSymbolWidth=60
StabsType=2

Example for Coff/Stabs (using Ticoff reader)

[ReadersTicoff]
C
C
MaxSymbolWidth=60
StabsType=2

Example for Ticoff

[ReadersTicoff]
C
C
MaxSymbolWidth=60
ReadOnlyTicoffPage=4
AppendTicoffPage=1
User-Defined Symbols

“To Create User-Defined Symbols” on page 109
“To Replace User-Defined Symbols” on page 109
“To Delete User-Defined Symbols” on page 110
“To Load User-Defined Symbols” on page 110

To Create User-Defined Symbols

1. Under the Symbol tab, select the User Defined tab.
2. Select the label name you want to define symbols for.
3. At the bottom of the User Defined tab, enter a symbol name in the entry field.
4. Select a numeric base.
5. Select Pattern or Range type for the symbol.
6. Enter values for the pattern or range the symbol will represent.
7. Select the Add button.
8. Repeat steps 3 through 7 for additional symbols.
9. You can edit your list of symbols by using Replace (see page 109) and Delete (see page 110), if desired.

See Also

“Using Symbols In The Logic Analyzer” on page 111

To Replace User-Defined Symbols

1. Under the Symbol tab, select the User Defined tab.
2. Select the label you want to replace symbols for.
3. Select the symbol to replace.

4. At the bottom of the User Defined tab, modify the symbol name, numeric base, Pattern/Range type, and value, as desired.

5. Select the Replace button.

6. Repeat steps 3 through 5 to replace other symbols, if desired.

---

**To Delete User-Defined Symbols**

1. Under the Symbol tab, select the User Defined tab.

2. Select the label you want to delete symbols from.

3. Select the symbol to delete.

4. Select the Delete button.

5. Repeat steps 3 and 4 to delete other symbols, if desired.

---

**To Load User-Defined Symbols**

If you have already saved a configuration file, and the configuration included user-defined symbols, load the file with its symbols, as follows:

1. In the menu bar of your analyzer window, select File and then Load Configuration....

2. In the Load Configuration dialog, select the directory and filename to be loaded.

3. Select the target of the load operation.

4. Select the Load button. User-defined symbols that were resident in the logic analyzer when the configuration was saved are now loaded and ready to use.

**See Also**

“Using Symbols In The Logic Analyzer” on page 111
Using Symbols In The Logic Analyzer

The ways symbols can be used in the logic analyzer are listed below:

- “Using Symbols As Trigger Terms” on page 111
- “Using Symbols as Search Patterns in Listing Displays” on page 112
- “Using Symbols as Trigger Terms in the Source Viewer” on page 112
- “Using Symbols as Pattern Filter Terms” on page 112
- “Using Symbols as Ranges in the Software Performance Analyzer” on page 113
- “Displaying Data in Symbolic Form” on page 96

Using Symbols As Trigger Terms

You can use either one or both types of symbols as terms within your trigger sequence:

- *Object File Symbols.*
- *User-Defined Symbols.*

1. At the bottom of the analyzer Trigger window, select the label button next to one of the resource terms, and choose Replace.

2. In the Resource selection dialog, select a label to be used in your trigger sequence.
   Use a label that has symbols loaded.

3. Set the numeric base of the trigger term to Symbols or Line #s.

4. Select the button to the right of the numeric base field.

5. In the Symbol Selector (see page 113) dialog, select the symbol you want to use.

**NOTE:**

The values of object file symbols used as trigger terms are automatically updated when the object file symbols are reloaded (see page 97).
Using Symbols as Search Patterns in Listing Displays

1. Under the Search tab in the Listing display, select the Advanced searching button.
2. In the Goto Pattern dialog, select the Define button.
3. In the Search Pattern dialog, select the Symbols numeric base.
4. Select Pattern, Range, Not Pattern, or Not Range.
5. Select the button to the right of the numeric base field.
6. In the Symbol Selector (see page 113) dialog, select the symbol you want to use.

See Also
Go to an Exact Pattern. (see the Listing Display Tool help volume)

Using Symbols as Trigger Terms in the Source Viewer

1. In the Source Viewer menu bar, select Trace, and select Trace Setup.
2. In the Source Line Trigger dialog, select Symbols or Line #s in the numeric base field.
3. Select Pattern, Range, Not Pattern, or Not Range.
4. Select the button to the right of the numeric base field.
5. In the Symbol Selector (see page 113) dialog, select the symbol you want to use.

See Also
To modify the trace setup. (see the Listing Display Tool help volume)

Using Symbols as Pattern Filter Terms

1. Select the numeric base field beside the selected filter term, and select
Chapter 1: Agilent Technologies 16557D 140MHz State/500MHz Timing Logic Analyzer

Using Symbols In The Logic Analyzer

Symbols or Line #s.

2. Select Pattern, Range, Not Pattern, or Not Range.

3. Select Remove Matching Data or Pass Matching Data, as desired.

4. Select the Absolute XXXX button.

5. In the Symbol Selector (see page 113) dialog, select the symbol you want to use.

Using Symbols as Ranges in the Software Performance Analyzer

1. In the state interval SPA tool, select the Symbols button in the Define Ranges dialog.

2. In the Symbol Selector (see page 114) dialog, select the symbol or group of symbols you want to use as ranges in your measurement.

See Also

Defining State Interval Ranges. (see the System Performance Analyzer help volume)

Using the Symbol Selector Dialog

1. In the Symbol Selector dialog, select the symbol you want to use. All of your symbols for the current label, regardless of type, will be available in the dialog.

   • Use the Search Pattern (see page 114) field to filter the list of symbols by name. You can use the Recall button to recall a desired Search Pattern.

   • Use the Find Symbols of Type selections to filter the symbols by type.

2. Select the symbol you want to use in the list of Matching Symbols.

3. If you are using object file symbols, you may need to:

   • Set Offset By (see page 115) to compensate for microprocessor prefetches.

   • Set Align to x Byte (see page 115) to trigger on odd-byte boundaries.
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Using Symbols In The Logic Analyzer

4. Select the Beginning, End, or Range of the symbol.

5. Select the OK button.
   The name of your symbol now appears as the value of the resource term.

6. Select the Cancel button to exit the Symbol Selector dialog without selecting a symbol.

Using the Symbol Selector Dialog

1. In the Symbol Selector dialog, select the symbol you want to use. All of
   your symbols, regardless of type, will be available in the dialog.
   - Use the Search Pattern (see page 114) field to filter the list of symbols
     by name. You can use the Recall button to recall a desired Search
     Pattern.
   - Use the Find Symbols of Type selections to filter the symbols by type.

2. Drag to select the symbols you want to use in the list of Matching
   Symbols.
   - Select the Select All button to select all symbols in the list.
   - Select the Unselect All button to unselect all symbols in the list.

3. Select the Add Selected Symbols To Range List button to place the
   selected symbols into the Current ranges list in the Define Ranges dialog.

4. Select the Close button to exit the Symbol Selector dialog.

Search Pattern

Use this field to locate particular symbols in the symbol databases. To
use this field, enter the name of a file or symbol. The system searches
the symbol database for symbols that match this name. Symbols that
match appear in the list of Matching Symbols. You can also use
wildcard characters to find symbols.

Asterisk wildcard (*)

The asterisk wildcard represents "any characters." When you perform a
search on the symbol database using just the asterisk, you will see a list
of all symbols contained in the database. The asterisk can also be
added to a search word to find all symbols that begin or end with the
same letters. For example, to find all of the symbols that begin with the letters "st", select the Search Pattern field and enter "st*".

**Align to x Byte Option**

Most processors do not fetch instructions from memory on byte boundaries. In order to trigger a logic analyzer on a symbol at an odd-numbered address, the address must be masked off. The "Align to x Byte" option allows you to mask off an address.

**Example**

Assume the symbol "main" occurs at address 100F. The processor being probed is a 68040, which fetches instructions on long-word (4-byte) boundaries. In order to trigger on address 100F, the Align to x Byte option sets the two least-significant address bits to "don't cares". This qualifies any address from 100C through 100F.

**Offset By Option**

The Offset By option allows you to add an offset value to the starting point of the symbol that you want to use as a term. You might do this in order to trigger on a point in a function that is beyond the preamble of the function, or to trigger on a point that is past the prefetch depth of the processor. Setting an offset helps to avoid false triggers in these situations. The offset specified in the Offset By field is applied before the address masking is done by the "Align to x Byte" option.

**Example**

An 80386 processor has a prefetch depth of 16 bytes. Assume functions `func1` and `func2` are adjacent to each other in physical memory, with `func2` following `func1`. In order to trigger on `func2` without getting a false trigger from a prefetch beyond the end of `func1`, you need to add an offset value to your trigger term. The offset value must be equal to or greater than the prefetch depth of the processor. In this case, you would add an offset of 16 bytes to your trigger term. You would set the value of the "Offset By" field to 10 hex. Now, when you specify `func2` as your trigger term, the logic analyzer will trigger on address `func2+10`. 
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Using Symbols In The Logic Analyzer
Glossary

**absolute**  Denotes the time period or count of states between a captured state and the trigger state. An absolute count of -10 indicates the state was captured ten states before the trigger state was captured.

**acquisition**  Denotes one complete cycle of data gathering by a measurement module. For example, if you are using an analyzer with 128K memory depth, one complete acquisition will capture and store 128K states in acquisition memory.

**analysis probe**  A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Also called a "preprocessor".

**analyzer 1**  In a logic analyzer with two machines, refers to the machine that is on by default. The default name is Analyzer<N>, where N is the slot letter.

**analyzer 2**  In a logic analyzer with two machines, refers to the machine that is off by default. The default name is Analyzer<N2>, where N is the slot letter.

**arming**  An instrument tool must be armed before it can search for its trigger condition. Typically, instruments are armed immediately when Run or Group Run is selected. You can set up one instrument to arm another using the Intermodule Window. In these setups, the second instrument cannot search for its trigger condition until it receives the arming signal from the first instrument. In some analyzer instruments, you can set up one analyzer machine to arm the other analyzer machine in the Trigger Window.

**asterisk (*)**  See edge terms, glitch, and labels.

**bits**  Bits represent the physical logic analyzer channels. A bit is a channel that has or can be assigned to a label. A bit is also a position in a label.

**card**  This refers to a single instrument intended for use in the Agilent Technologies 16600A-series or 16700A/B-series mainframes. One card fills one slot in the mainframe. A module may comprise a single card or multiple cards cabled together.

**channel**  The entire signal path from the probe tip, through the cable and module, up to the label grouping.

**click**  When using a mouse as the pointing device, to click an item, position the cursor over the item.
Then quickly press and release the *left mouse button*.

**clock channel** A logic analyzer *channel* that can be used to carry the clock signal. When it is not needed for clock signals, it can be used as a *data channel*, except in the Agilent Technologies 16517A.

**context record** A context record is a small segment of analyzer memory that stores an event of interest along with the states that immediately preceded it and the states that immediately followed it.

**context store** If your analyzer can perform context store measurements, you will see a button labeled *Context Store* under the Trigger tab. Typical context store measurements are used to capture writes to a variable or calls to a subroutine, along with the activity preceding and following the events. A context store measurement divides analyzer memory into a series of context records. If you have a 64K analyzer memory and select a 16-state context, the analyzer memory is divided into 4K 16-state context records. If you have a 64K analyzer memory and select a 64-state context, the analyzer memory will be divided into 1K 64-state records.

**count** The count function records periods of time or numbers of state transactions between states stored in memory. You can set up the analyzer count function to count occurrences of a selected event during the trace, such as counting how many times a variable is read between each of the writes to the variable. The analyzer can also be set up to count elapsed time, such as counting the time spent executing within a particular function during a run of your target program.

**cross triggering** Using intermodule capabilities to have measurement modules trigger each other. For example, you can have an external instrument arm a logic analyzer, which subsequently triggers an oscilloscope when it finds the trigger state.

**data channel** A *channel* that carries data. Data channels cannot be used to clock logic analyzers.

**data field** A data field in the pattern generator is the data value associated with a single label within a particular data vector.

**data set** A data set is made up of all labels and data stored in memory of any single analyzer machine or instrument tool. Multiple data sets can be displayed together when...
sourced into a single display tool. The Filter tool is used to pass on partial data sets to analysis or display tools.

**debug mode**  See monitor.

**delay**  The delay function sets the horizontal position of the waveform on the screen for the oscilloscope and timing analyzer. Delay time is measured from the trigger point in seconds or states.

**demo mode**  An emulation control session which is not connected to a real target system. All windows can be viewed, but the data displayed is simulated. To start demo mode, select Start User Session from the Emulation Control Interface and enter the demo name in the Processor Probe LAN Name field. Select the Help button in the Start User Session window for details.

**deskewing**  To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is normally done by routing a single test signal to the inputs of two different modules, then adjusting the Intermodule Skew so that both modules recognize the signal at the same time.

**don't care**  For terms, a "don't care" means that the state of the signal (high or low) is not relevant to the measurement. The analyzer ignores the state of this signal when determining whether a match occurs on an input label. "Don't care" signals are still sampled and their values can be displayed with the rest of the data. Don't cares are represented by the X character in numeric values and the dot (.) in timing edge specifications.

**dot (.)**  See edge terms, glitch, labels, and don't care.

**double-click**  When using a mouse as the pointing device, to double-click an item, position the cursor over the item, and then quickly press and release the left mouse button twice.

**drag and drop**  Using a Mouse:
Position the cursor over the item, and then press and hold the left mouse button down, move the mouse to drag the item to a new location. When the item is positioned where you want it, release the mouse button.

Using the Touchscreen:
Position your finger over the item, then press and hold finger to the screen. While holding the finger down, slide the finger along the screen dragging the item to a new
location. When the item is positioned where you want it, release your finger.

**edge mode** In an oscilloscope, this is the trigger mode that causes a trigger based on a single channel edge, either rising or falling.

**edge terms** Logic analyzer trigger resources that allow detection of transitions on a signal. An edge term can be set to detect a rising edge, falling edge, or either edge. Some logic analyzers can also detect no edge or a glitch on an input signal. Edges are specified by selecting arrows. The dot (.) ignores the bit. The asterisk (*) specifies a glitch on the bit.

**emulation module** A module within the logic analysis system mainframe that provides an emulation connection to the debug port of a microprocessor. An E5901A emulation module is used with a target interface module (TIM) or an analysis probe. An E5901B emulation module is used with an E5900A emulation probe.

**emulation probe** The stand-alone equivalent of an emulation module. Most of the tasks which can be performed using an emulation module can also be performed using an emulation probe connected to your logic analysis system via a LAN.

**emulator** An emulation module or an emulation probe.

**Ethernet address** See link-level address.

**events** Events are the things you are looking for in your target system. In the logic analyzer interface, they take a single line. Examples of events are Label1 = XX and Timer 1 > 400 ns.

**filter expression** The filter expression is the logical OR combination of all of the filter terms. States in your data that match the filter expression can be filtered out or passed through the Pattern Filter.

**filter term** A variable that you define in order to specify which states to filter out or pass through. Filter terms are logically OR’ed together to create the filter expression.

**Format** The selections under the logic analyzer Format tab tell the logic analyzer what data you want to collect, such as which channels represent buses (labels) and what logic threshold your signals use.
frame  The Agilent Technologies 16600A-series or 16700A/B-series logic analysis system mainframe. See also logic analysis system.

gateway address  An IP address entered in integer dot notation. The default gateway address is 0.0.0.0, which allows all connections on the local network or subnet. If connections are to be made across networks or subnets, this address must be set to the address of the gateway machine.

glitch  A glitch occurs when two or more transitions cross the logic threshold between consecutive timing analyzer samples. You can specify glitch detection by choosing the asterisk (*) for edge terms under the timing analyzer Trigger tab.

grouped event  A grouped event is a list of events that you have grouped, and optionally named. It can be reused in other trigger sequence levels. Only available in Agilent Technologies 16715A, 16716A, and 16717A logic analyzers.

held value  A value that is held until the next sample. A held value can exist in multiple data sets.

immediate mode  In an oscilloscope, the trigger mode that does not require a specific trigger condition such as an edge or a pattern. Use immediate mode when the oscilloscope is armed by another instrument.

interconnect cable  Short name for module/probe interconnect cable.

intermodule  Intermodule is a term used when multiple instrument tools are connected together for the purpose of one instrument arming another. In such a configuration, an arming tree is developed and the group run function is designated to start all instrument tools. Multiple instrument configurations are done in the Intermodule window.

intermodule bus  The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to arm another. Data acquired by instruments using the IMB is time-correlated.

internet address  Also called Internet Protocol address or IP address. A 32-bit network address. It is usually represented as decimal numbers separated by periods; for example, 192.35.12.6. Ask your LAN administrator if you need an internet address.
Glossary

labels  Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits. Labels are created in the Format tab.

line numbers  A line number (Line #s) is a special use of symbols. Line numbers represent lines in your source file, typically lines that have no unique symbols defined to represent them.

link-level address  Also referred to as the Ethernet address, this is the unique address of the LAN interface. This value is set at the factory and cannot be changed. The link-level address of a particular piece of equipment is often printed on a label above the LAN connector. An example of a link-level address in hexadecimal: 0800090012AB.

local session  A local session is when you run the logic analysis system using the local display connected to the product hardware.

logic analysis system  The Agilent Technologies 16600A-series or 16700A/B-series mainframes, and all tools designed to work with it. Usually used to mean the specific system and tools you are working with right now.

machine  Some logic analyzers allow you to set up two measurements at the same time. Each measurement is handled by a different machine. This is represented in the Workspace window by two icons, differentiated by a 1 and a 2 in the upper right-hand corner of the icon. Logic analyzer resources such as pods and trigger terms cannot be shared by the machines.

markers  Markers are the green and yellow lines in the display that are labeled x, o, G1, and G2. Use them to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of states in the data. The x and o markers are local to the immediate display, while G1 and G2 are global between time correlated displays.

master card  In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16555D would be referred to as Slot C: machine because the master card is in slot C of the mainframe. The other cards of the module are called expansion cards.
Glossary

**menu bar**  The menu bar is located at the top of all windows. Use it to select *File* operations, tool or system *Options*, and tool or system level *Help*.

**message bar**  The message bar displays mouse button functions for the window area or field directly beneath the mouse cursor. Use the mouse and message bar together to prompt yourself to functions and shortcuts.

**module**  An instrument that uses a single timebase in its operation. Modules can have from one to five cards functioning as a single instrument. When a module has more than one card, system window will show the instrument icon in the slot of the master card.

**module/probe interconnect cable**

The module/probe interconnect cable connects an E5901B emulation module to an E5900B emulation probe. It provides power and a serial connection. A LAN connection is also required to use the emulation probe.

**monitor**  When using the Emulation Control Interface, running the monitor means the processor is in debug mode (that is, executing the debug exception) instead of executing the user program.

**panning**  The action of moving the waveform along the timebase by varying the delay value in the Delay field. This action allows you to control the portion of acquisition memory that will be displayed on the screen.

**pattern mode**  In an oscilloscope, the trigger mode that allows you to set the oscilloscope to trigger on a specified combination of input signal levels.

**pattern terms**  Logic analyzer resources that represent single states to be found on labeled sets of bits; for example, an address on the address bus or a status on the status lines.

**period (.)**  See *edge terms*, *glitch*, *labels*, and *don't care*.

**pod**  See *pod pair*

**pod pair**  A group of two pods containing 16 channels each, used to physically connect data and clock signals from the unit under test to the analyzer. Pods are assigned by pairs in the analyzer interface. The number of pod pairs available is determined by the channel width of the instrument.
point  To point to an item, move the mouse cursor over the item, or position your finger over the item.

preprocessor  See analysis probe.

primary branch  The primary branch is indicated in the Trigger sequence step dialog box as either the Then find or Trigger on selection. The destination of the primary branch is always the next state in the sequence, except for the Agilent Technologies 16517A. The primary branch has an optional occurrence count field that can be used to count a number of occurrences of the branch condition. See also secondary branch.

probe  A device to connect the various instruments of the logic analysis system to the target system. There are many types of probes and the one you should use depends on the instrument and your data requirements. As a verb, "to probe" means to attach a probe to the target system.

processor probe  See emulation probe.

range terms  Logic analyzer resources that represent ranges of values to be found on labeled sets of bits. For example, range terms could identify a range of addresses to be found on the address bus or a range of data values to be found on the data bus. In the trigger sequence, range terms are considered to be true when any value within the range occurs.

relative  Denotes time period or count of states between the current state and the previous state.

remote display  A remote display is a display other than the one connected to the product hardware. Remote displays must be identified to the network through an address location.

remote session  A remote session is when you run the logic analyzer using a display that is located away from the product hardware.

right-click  When using a mouse for a pointing device, to right-click an item, position the cursor over the item, and then quickly press and release the right mouse button.

sample  A data sample is a portion of a data set, sometimes just one point. When an instrument samples the target system, it is taking a single measurement as part of its data acquisition cycle.

Sampling  Use the selections under
the logic analyzer Sampling tab to tell the logic analyzer how you want to make measurements, such as State vs. Timing.

**secondary branch** The secondary branch is indicated in the Trigger sequence step dialog box as the *else on* selection. The destination of the secondary branch can be specified as any other active sequence state. See also *primary branch*.

**session** A session begins when you start a *local session* or *remote session* from the session manager, and ends when you select *Exit* from the main window. Exiting a session returns all tools to their initial configurations.

**skew** Skew is the difference in channel delays between measurement channels. Typically, skew between modules is caused by differences in designs of measurement channels, and differences in characteristics of the electronic components within those channels. You should adjust measurement modules to eliminate as much skew as possible so that it does not affect the accuracy of your measurements.

**state measurement** In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

**store qualification** Store qualification is only available in a *state measurement*, not *timing measurements*. Store qualification allows you to specify the type of information (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as no-ops or wait-loops. To set up store qualification, use the *While storing* field in a logic analyzer trigger sequence dialog.

**subnet mask** A subnet mask blocks out part of an IP address so that the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.255.0. Ask your LAN administrator if you need a the subnet mask for your network.

**symbols** Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of
symbols are available:

- **Object file symbols** - Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.

- **User-defined symbols** - Symbols you create.

Symbols can be used as *pattern* and *range* terms for:

- Searches in the listing display.
- Triggering in logic analyzers and in the source correlation trigger setup.
- Qualifying data in the filter tool and system performance analysis tool set.

**system administrator** The system administrator is a person who manages your system, taking care of such tasks as adding peripheral devices, adding new users, and doing system backup. In general, the system administrator is the person you go to with questions about implementing your software.

**target system** The system under test, which contains the microprocessor you are probing.

**terms** Terms are variables that can be used in trigger sequences. A term can be a single value on a label or set of labels, any value within a range of values on a label or set of labels, or a glitch or edge transition on bits within a label or set of labels.

**TIM** A TIM (Target Interface Module) makes connections between the cable from the emulation module or emulation probe and the cable to the debug port on the system under test.

**timer terms** Logic analyzer resources that are used to measure the time the trigger sequence remains within one sequence step, or a set of sequence steps. Timers can be used to detect when a condition lasts too long or not long enough. They can be used to measure pulse duration, or duration of a wait loop. A single timer term can be used to delay trigger until a period of time after detection of a significant event.

**time-correlated** Time correlated measurements are measurements involving more than one instrument in which all instruments have a common time or trigger reference.

**timing measurement** In a timing measurement, the logic analyzer samples data at regular intervals.
Glossary

accord to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. These measurements are asynchronous with the test system.

tools A tool is a stand-alone piece of functionality. A tool can be an instrument that acquires data, a display for viewing data, or a post-processing analysis helper. Tools are represented as icons in the main window of the interface.

toolbox The Toolbox is located on the left side of the main window. It is used to display the available hardware and software tools. As you add new tools to your system, their icons will appear in the Toolbox.

tool icon Tool icons that appear in the workspace are representations of the hardware and software tools selected from the toolbox. If they are placed directly over a current measurement, the tools automatically connect to that measurement. If they are placed on an open area of the main window, you must connect them to a measurement using the mouse.

trace See acquisition.

trigger Trigger is an event that occurs immediately after the instrument recognizes a match between the incoming data and the trigger specification. Once trigger occurs, the instrument completes its acquisition, including any store qualification that may be specified.

trigger sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to trigger.

trigger specification A trigger specification is a set of conditions that must be true before the instrument triggers.

workspace The workspace is the large area under the message bar and to the right of the toolbox. The workspace is where you place the different instrument, display, and analysis tools. Once in the workspace, the tool icons graphically represent a complete picture of the measurements.

zooming In the oscilloscope or timing analyzer, to expand and contract the waveform along the time base by varying the value in the s/Div field. This action allows you to select specific portions of a particular
waveform in acquisition memory that will be displayed on the screen. You can view any portion of the waveform record in acquisition memory.
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